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Page No.	Issue
*Title	9 Oct. 61
*i thru iii	22 June 62
*iv	22 June 62
1-1	Original
*1-2	22 June 62
*2-1, 2-2	22 June 62
*3-1	22 June 62
*3-2, 3-3	22 June 62
*3-4	22 June 62
*3-5, 3-6	22 June 62
3-7	Original
3-8	Blank
*3-9	22 June 62
*3-10, 3-11	22 June 62
3-12	Blank
*3-13	15 June 61
3-14	Blank
*3-15	22 June 62
3-16	Blank
3-17	Original
3-18	Blank
*3-19 thru 3-21	Original
*4-1, 4-2	22 June 62
5-1	Original
5-2	Blank
6-1	Original
7-1	Original
*7-3 thru 7-7	15 June 61
*7-2, 7-8 thru 7-12	22 June 62
*7-13 thru 7-19	15 June 61
*7-20 thru 7-22	Original
8-1	Original
8-2	Blank
*8-3	22 June 62
*8-4, 8-5	15 June 61
*8-6, 8-7	22 June 62
*8-8	15 June 61
*8-9, 8-10, 8-11	22 June 62
*8-12	15 June 61
*8-13 thru 8-16	22 June 62
*8-17 thru 8-31	15 June 61
8-32	Blank
9-1	Original
9-2	Blank
9-3	Original
9-4	Blank
9-5	Original
9-6	Blank
*9-7	15 June 61
9-8	Blank
*9-9	15 June 61
9-10	Blank
*9-11	15 June 61
9-12	Blank
*9-13	15 June 61
9-14	Blank
9-15	Original
9-16	Blank
9-17	Original
9-18	Blank
*9-19	15 June 61
9-20	Blank
*9-21	15 June 61
9-22	Blank
*9-23	15 June 61
9-24	Blank
9-25	Original
9-26	Blank
*9-27	15 June 61
9-28	Blank
9-29	Original
9-30	Blank
9-31	Original
9-32	Blank
*9-33	Original
9-34	Blank
*9-35	Original
9-36	Blank
*9-37	Original
9-38	Blank
Appendix	
*Title Page 1A	15 June 61
Page 1 of 7 thru 7 of 7	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 2	Original
*Page 2 of 2	15 June 61
Page 1 of 2 thru 2 of 2	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 3 thru 3 of 3	Original
*Page 1 of 2	31 July 61
Page 2 of 2	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 2 thru 2 of 2	Original
*Page 1 of 2 thru 2 of 2	Original
*Page 1 of 8	15 June 61
Pages 2, 3 of 8	Original
*Page 4 of 8	15 June 61
Pages 5 thru 8 of 8	Original
*Pages 1 thru 13	Original
Addendum	
*10-1	Original
*10-2	Original

*The asterisk indicates pages changed, added or deleted by the current change.

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

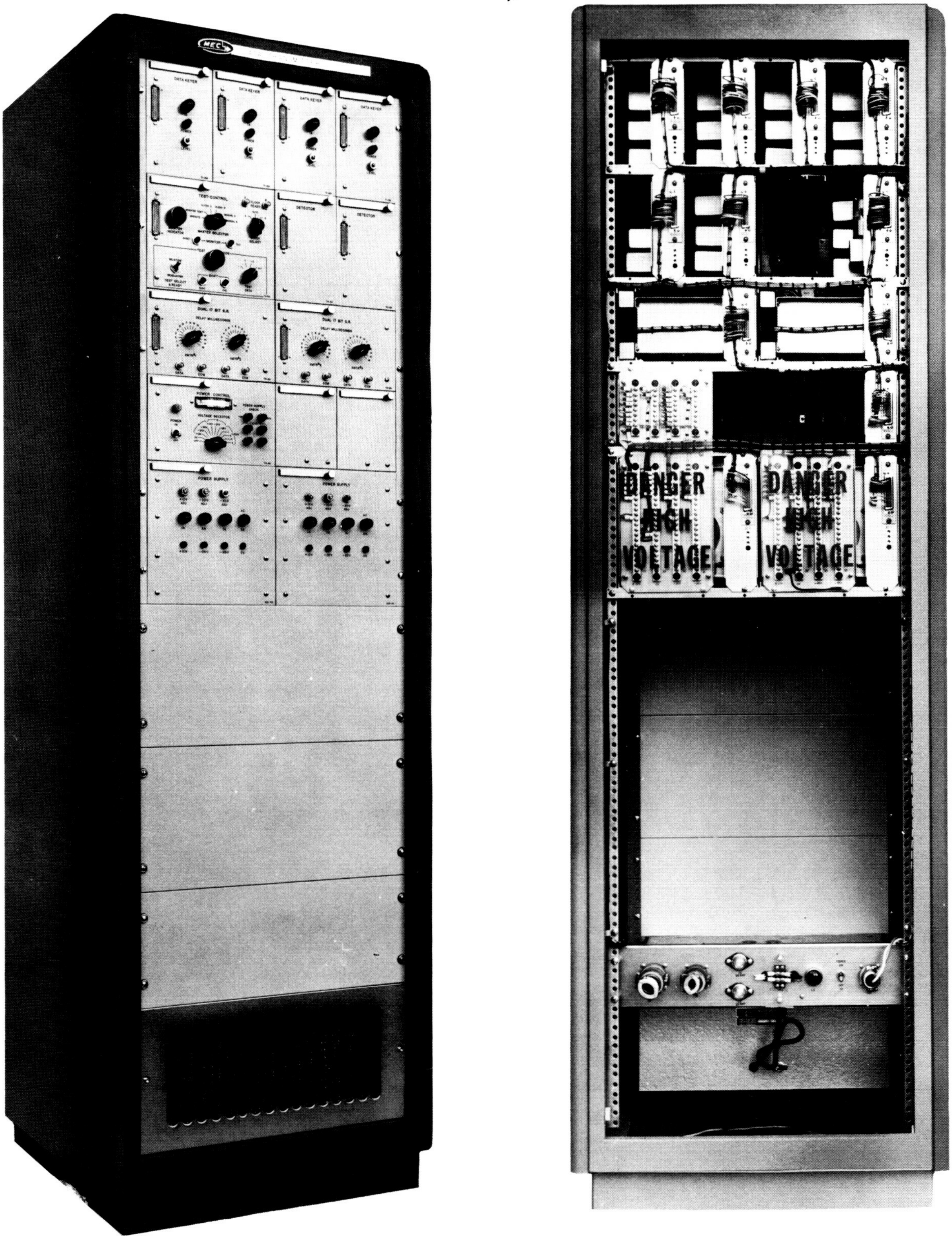


Figure 1-1. MEC Model 74 Data Transmitter

CHAPTER I

INTRODUCTION

1-1. PURPOSE OF EQUIPMENT

The Milgo Electronic Corporation (MEC) Model 74 Data Transmitter receives digital information and control signals from a Data Communication Channel (DCC), formerly referred to as a Real Time Channel (RTC). The Transmitter accepts this information one bit at a time in a serial format and converts it into keyed tone bursts, which are transmitted over 3kc telephone voice lines. In normal operation, the Transmitter works in conjunction with the MEC Model 75 Data Receiver. Provisions are made within the Transmitter for several test modes of operation so that the Transmitter and other associated equipment, can be tested either with or without using the DCC.

1-2. SCOPE OF MANUAL

This instruction manual describes the MEC Model 74 Data Transmitter, designed and manufactured by MEC, for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

1-3. PURPOSE OF MANUAL

This instruction manual is provided as an aid to better understanding of the operation and theory of the MEC Model 74 Data Transmitter and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations. It is necessary that the operator, or any person involved in the operation of this equipment, thoroughly read and fully understand the contents of this manual.

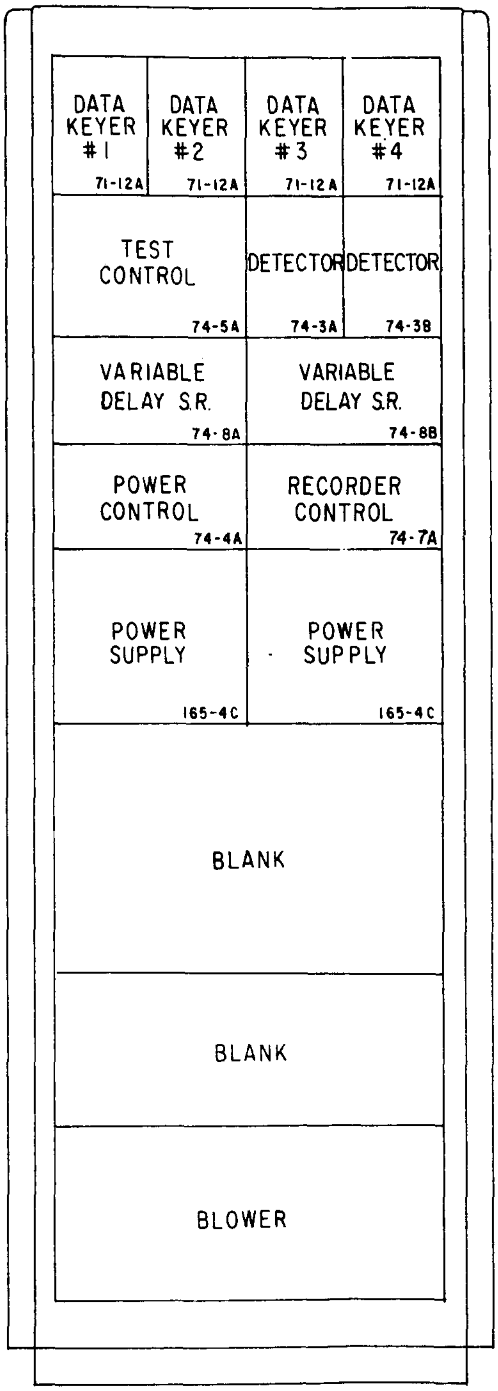


Figure 1-2. MEC Model 74 Data Transmitter Chassis Arrangement

CHAPTER II
GENERAL DESCRIPTION

2-1. GENERAL

2-1.1. The MEC Model 74 Data Transmitter receives digital information one bit at a time in a serial format from a DCC and converts this information into keyed tone bursts. These tone bursts are then transmitted over a 3 kc telephone voice line.

2-1.2. The Data Transmitter generates four outputs.

a. A tone representing data.

b. A tone burst representing End of Word.

c. A tone burst representing Start of Word.

d. A pulse which signals the DCC to send the next bit of data.

2-3. PHYSICAL DESCRIPTION

The Data Transmitter is contained in a standard MEC type 4 1F rack. This rack is 74 1/8 inches high, 22 inches deep, and 19 1/16 inches wide. The weight of the complete Transmitter is approximately 500 pounds. All chassis are of modular construction and employ 50-pin connectors to effect the connection of each chassis to the rack wiring. The location of each chassis is illustrated in Figure 1-2.

2-3. DATA COMMUNICATION CHANNEL OPERATION

2-3.1. The DCC sends two lines of information to the Transmitter: one line is for data transfer, the other is a control signal to indicate that data is available.

2-3.1.1. The select and ready line is a signal for the Transmitter to send a SOW tone burst and to start sampling the data line. The fall of select and ready is a signal to send an EOW tone burst.

2-3.1.2. The data line is that portion of the output of the DCC that is to be transformed into tone bursts for transmission.

2-3.2. The DCC receives a shift request pulse from the Transmitter, which requests the next data bit.

2-4. INPUTS

2-4.1. Signal Inputs - The Model 74 Data Transmitter receives information from the DCC through J17 at the rear of the rack. Select and ready enters J17 through pin C. When the Transmitter is selected, the received level is 8 volts ±0.5 volts. When the Transmitter is deselected, the received level is 0 volts ±0.5 volts. Data levels are 8 volts ±0.5 volts for a "1", and 0 volts ±0.5 volts for a "0". The data level is achieved within 10 microseconds of the select and ready line, and attains the next data bit level within 10 microseconds after the previous shift request.

2-4.2. Power Inputs - The Transmitter receives a-c power through J15 at the rear of the rack. It operates on 120 vac, 60 cycles, ±10% at less than 10 amperes.

2-5. OUTPUTS

2-5.1. The shift request output to the DCC is a 10-microsecond pulse, sent out through J17, pin A. It is a positive-going pulse, going from approximately -10 volts to 0 volts. A "0" is approximately -10 volts, and a "1" is 0 volts.

2-5.2. The Transmitter has 4 isolated outputs that feed 600-ohm transmission lines. Each of these outputs is adjustable from -30dbm to +10dbm. The table below shows the pin numbers of J16 that the outputs are routed to.

Keyer	Pin
1	A and C
2	E and G
3	J and L
4	N and U

CHAPTER III

THEORY OF OPERATION

3-1. GENERAL

3-1.1. The MEC Model 74 Data Transmitter is designed to accept digital information serially, and transmit it serially over 600 ohm 3kc telephone lines at a 1kc bit rate. The Transmitter consists of circuitry which accepts one source of information, and converts it into a form suitable for driving four independent Keyers that transmit information over four separate telephone lines. It accepts one line of data from a DCC and drives two Detectors in parallel. Each Detector inserts information into a variable Delay Shift Register. Although each Shift Register drives two Keyer Chassis, the input to each Keyer is taken from the Delay Shift Registers independently, thereby delaying the information to each Keyer independently.

3-1.2. For increased reliability, the Data Transmitter contains two MEC Model 165-4C Power Supplies. These supplies are isolated from each other, and should a failure occur in one supply, it will not place an additional load on the remaining supply. Power Supply A is the source for one-half of the system consisting of the one-half of the Test-Control Chassis, Detector A, one Delay Shift Register, and Data Keyers #1 and #2. Power Supply B controls the second half consisting of the other half of the Test-Control Chassis, Detector B, the other Delay Shift Register, and Data Keyers #3 and #4.

3-1.3. The output of a Keyer Chassis is shown in Figure 9-15. Although the patterns shown are test patterns, the tone bursts are the same as those triggered by actual data.

3-2. OPERATE MODES

3-2.1. System Operation

3-2.1.1. Operation of the Data Transmitter is conducted in this mode, and all redundancies built into the system are in operation. The timing for the Transmitter is controlled by a 1 kc tuning fork in the Test-Control Chassis. In the case of a failure in the tuning fork or its associated circuitry another tuning fork is automatically switched into operation.

3-2.1.2. The data and select and ready lines are routed through the Test-Control Chassis into the two Detector Chassis. The data is processed in the Detector Chassis and sent to the Delay Shift Registers. Once the data has been delayed, by the amount of time selected by the operator, the data and EOW signals are fed into the Keyers, where they emerge as tone bursts for transmission.

3-2.2. Loop Test Operation - This Model is used to test the MEC Model 74 and the MEC Model 72 Data Receiver simultaneously. The output of the Model 74 Data Transmitter is fed directly into the Model 74 Data Receiver and data is fed back into Computer for comparing itagainst the data sent by the Computer. The MEC Model 74 Transmitter is placed in the OPERATE mode for this test.

MASTER SELECTOR Switch, S506, is in the OPERATE position.

3-3. TEST MODES

3-3.1. Monitor Test - This test mode is similar to the operate mode, except for the inputs to the Transmitter. Both the select and ready level and the data pattern are generated internally in the Transmitter. (Select and ready is cycled approximately once every 700 milliseconds. The data pattern is controlled by the TEST DATA switch, S507, on the front panel of the Test Control Chassis.) In this mode the monitor circuit may be tested by closing the MONITOR TEST switch, S505, on the front panel of the Test Control Chassis. This switch interrupts the output of Clock A, enabling the operator to ascertain if Clock B gains control of the Transmitter. If this is the case, the RESET pushbutton, S503, should be pressed to place the Transmitter under the control of Clock A.

3-3.2. Clock A - In this test mode, Clock B is disconnected and Clock A is locked into control. Select and ready is cycled approximately once every 700 milliseconds, and the data pattern is controlled by the TEST DATA switch.

3-3.3. Clock B - This test mode is similar to the preceding test mode except that Clock B is locked into control.

3-3.4. Manual A - This test mode allows for manual insertion of data, bit by bit. Select and ready is controlled by the TEST SELECT & READY toggle switch, S504. Data is controlled by two pushbuttons on the front panel of the Test Control Chassis. Pushbutton, S501, inserts "1"s, and pushbutton, S502, inserts "0"s. In this mode, both clocks are disconnected, but the data entry and shifting is entered through the circuitry normally controlled by Clock A.

3-3.5. Manual B - This test mode is the same as Manual A except that data entry and shifting is entered through the circuitry normally controlled by Clock B.

3-4. TEST CONTROL CHASSIS, MEC MODEL 74-5A (Figures 3-1, 9-3 and 9-4)

3-4.1. Operate Mode

3-4.1.1. The Test-Control Chassis provides the control and test functions for driving the Transmitter. In the operate mode, the MASTER SELECTOR switch, S506, is in the OPERATE position. Select and ready enters the chassis on pin 3, is routed through S506D, and leaves the chassis on pins 6 and 7 to the Detectors. Data enters on pin 4, is routed through S506E, and leaves the chassis on pins 8 and 9 to the Detectors.

3-4.1.2. TF501 and TF502 are 1 kc tuning forks. These tuning forks drive into N505 and N508 respectively, which amplify and square the signals and provide positive feedback to the tuning forks to sustain oscillation. The outputs of N505 and N508 are the triggers for N506 and N509, two 200 microsecond one-shots, which are used to trigger three circuits in each Detector. On the leading edge of the one-shot (Figure 9-15, waveform a.), a trigger is sent to generate a shift request pulse which is then sent back to the DCC to request the next data bit. (The first shift request pulse, generated after the rise of select and ready is blocked from the DCC; this insures that the first data bit is sampled.) The shift request pulse generated in Detector A is monitored by a circuit which drives relay K501. When this shift request pulse is being generated, K501 is energized, and the outputs of N509 drive the Transmitter. If the shift request pulse fails, K501 drops out and the outputs of N506 drive the Transmitter. The shift request pulse coming from Detector B now goes to the DCC.

3-4.1.3. Two other triggers exist in addition to the shift request triggers sent to each Detector. One is sent to each Detector to generate a sample pulse (Figure 9-15, waveform b.), and one is sent to each Shift Register Chassis to trigger the core drivers (Figure 9-15, waveform c.). These two latter triggers are sent to the other chassis after passing through K501. This action results in only one clock driving the Transmitter. The timing sequence is such that a shift request pulse occurs simultaneously with the core shift, and data is sampled 200 microseconds later. (See Figure 9-2, Timing Diagram.)

3-4.1.4. The CLOCK SELECT switch, S508, is a manual override switch for the monitor circuit. If the monitor should fail during operation, and one of the clocks should also fail, the operator can give control of the system to either clock. The clock ready lights, DS501 and DS502, are on when their respective clocks are operating. Switch S508 is connected into the relay circuitry only in the operate mode. The MONITOR INDICATOR, I501, is connected through relay K501. This indicator will light whenever the relay is de-energized, giving the operator a clear indication of trouble. The indicator is also connected to the manual override switch. If the override is not in the AUTO position, the lamp will glow.

3-4.2. Monitor Test - The Model 74 Data Transmitter operates essentially the same in monitor test mode as in the operate mode, except that data is generated internally, as is select and ready. The shift request pulse is used by flip-flop N507 as a count input. The output of this counter is connected to the TEST DATA switch, S507. The output of N507 is a 20 volt square wave going from -20 volts to 0 volts. If a "1-0" pattern or a "0-1" pattern is selected, this square wave is fed into N501B and N502B, where the level is changed to 0 volts and +12 volts, respectively. If a "1" pattern is selected, the input to N501B is held at 0 volts. If a "0" pattern is selected, the input of N501B is controlled by a one-shot in the "B" detector chassis. (An all "0" test pattern actually contains a "1" approximately 100 microseconds after SOW and every 100 microseconds thereafter.) The output of N507 is also fed into the Detector B Chassis in order to reset the select and ready level at the correct time. Select and ready enters the Test-Control Chassis as a -20 volt level for approximately 100 milliseconds, followed by a 0 volt level for approximately 600 milliseconds. These levels are converted to a 0 volt and a +12 volt level, respectively in N501A and N502A. In the monitor test mode, switch S506 is connected in series with the output of N508. This allows Clock A to be interrupted, enabling Clock B to be switched in. The MONITOR RESET switch S503 must then be pushed to reset the monitor circuit at which time Clock A will resume control.

3-4.3. Clock A - In this test mode, Clock B is disconnected and Clock A is locked into control. The remainder of the chassis operates as it does in the monitor test mode.

3-4.4. Clock B - This test mode is similar to Clock A, except that Clock B is locked into control.

3-4.5. Manual A Test

3-4.5.1. In this test mode, both clocks are disconnected. Data and select and ready are controlled manually, data being controlled by the SHIFT ONE and SHIFT ZERO pushbuttons, S502 and S501, and the select and ready being controlled by toggle switch S504. When S504 is closed, relay K502 is closed and applies +12 volts to the select and ready lines. Switch S501 is pushed for a shift "1", which triggers one-shot N503. The output of this one-shot N509 and also holds the input to N501B at 9 volts, which is a "1" input. Switch S502 is pushed for a shift "0", which triggers one-shot N504. The output

3-4.5.2. In the Manual A mode, the outputs of N509 are reversed, providing a timing sequence of sample, then shift; rather than shift, then sample.

3-4.7. Manual B Test - This test mode operates in a similar manner as Manual A, except that N506 is triggered instead of N509.

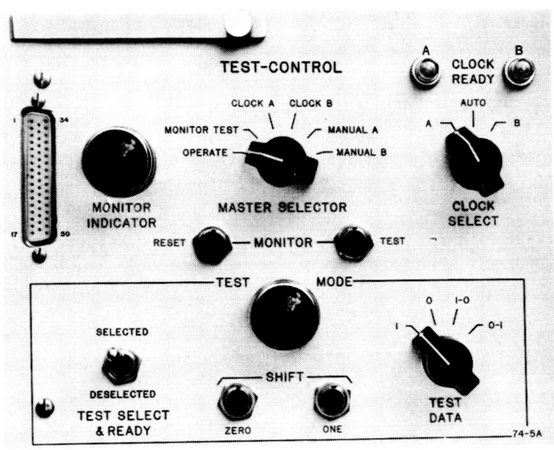


Figure 3-1. Test-Control Chassis

3-5. DETECTOR A CHASSIS, MEC MODEL 74-3A (Figures 3-2, 9-5 and 9-6)

3-5.1. General - The Detector A Chassis accepts information from the DCC, changes its form, and feeds it into the Delay Shift Register Chassis, which drives Transmitters 1 and 2. The Detector A chassis has six outputs: SOW pulses, data pulses, EOW pulses, artificial "1"s, shift request pulses, and a relay driving level for switching clocks in the Test Control Chassis.

3-5.2. SOW, EOW, Data Artificial "1" Circuitry

3-5.2.1. SOW is generated by N322, a 20 microsecond one-shot. When Select and Ready rises, it is inverted twice by N302A and N302B. The output of N302B (pin 5) is differentiated by C312 and R323. This output level is changed since R323 is referenced to -3.5. volts. The positive spike triggers N320, a TN90B flip-flop, causing pin 5 to go from -20 volts to 0 volts. The next shift request pulse from the Test Control Chassis now overcome the bias on CR324 and triggers N321, a 200 microsecond one-shot. When pin 5 of N320 is at -20 volts, the shift request pulse is not sufficient to overcome the bias on CR324 and N321 is not triggered. When N321 times out the pin 5 output goes from -20 volts to 0 volts and N322, a 20 microsecond one-shot is triggered, inserting a "1" in the SOW bank of cores in the Variable Delay Shift Register A. When N322 times out, the pin 5 output resets N320.

3-5.2.3. N313 is a 20 microsecond one-shot connected in series with the auxiliary winding of the first data core which is, in turn, connected to pin 6 of emitter follower N319 through diode CR312. Pin 6 of N319 is at -20 volts when the incoming data is at 8 volts, which is a "1" level. When N313 fires, pin 7 goes from -20 volts to 0 volts (Figure 9-15, waveform e.). Since pin 6 of N319 is at -20 volts for an incoming "1", current flows through the auxiliary winding, and a "1" is inserted. If the incoming data is a "0", pin 6 of N319 is at 0 volts and CR312 is back-biased. When N313 fires, pin 7 again rises to 0 volts, but no current flows in the auxiliary winding and a "0" is inserted. When select and ready falls, N311 is set, with pin 5 going to -20 volts and pin 8 going to 0 volts.

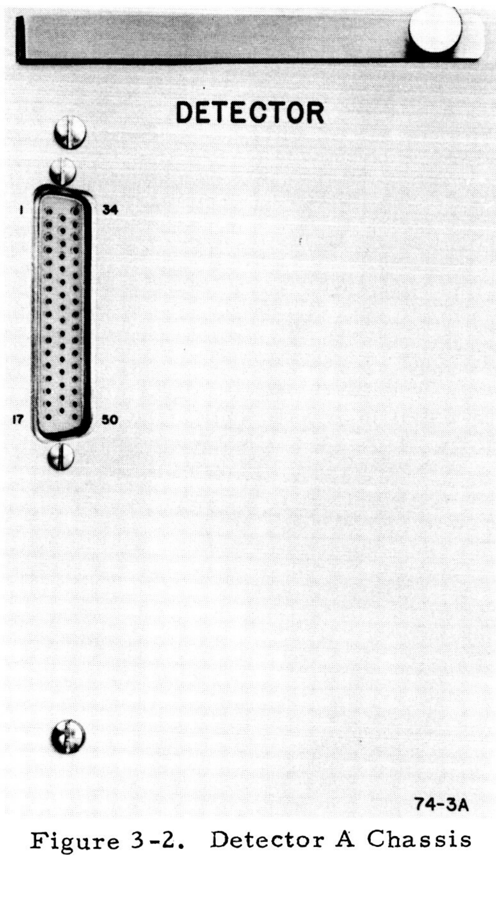


Figure 3-2. Detector A Chassis

3-5.2.4. The sample trigger is now steered away from N313, since CR306 is back biased, and is coupled to N308 through CR307. N308 is a 20 microsecond one-shot that is fed into the regular input of the first data core (Figure 9-15, waveform d.). Thus, when select and ready is down, artificial "1"s are generated and the data one-shot is disconnected. With the fall of select and ready, flip-flop N303 is set, causing pin 8 to go to 0 volts. This causes CR301 to be back biased by 2 volts.

3-5.2.5. When the first artificial "1" pulse is generated, it fires N304, a 20 microsecond one-shot. This pulse is inserted into the first core of the EOW Delay Shift Register, and also resets flip-flop N303. Pin 8 of N303 now goes to -20 volts, which back biases CR301, keeping N304 from firing again until select and ready rises and then falls. In this manner, only one EOW is generated per word.

3-5.2.6. Flip-flop N307 steers the shift trigger pulses. N307 is reset with the rise of select and ready, pin 5 going from -20 volts to 0 volts, and pin 8 going from 0 volts to -20 volts. CR304 is now back biased by 20 volts and CR303 is back biased by 2 volts. Since the shift trigger is less than 20 volts, CR304 will not open, however, CR303 allows the pulse to go through.

3-5.2.7. Flip-flops N309 and N310 are used as an anti-sliver circuit. When select and ready rises, N309 is reset, pin 5 going to 0 volts, and pin 8 going to -20 volts. N310 is in the set condition, with pin 5 at -20 volts. The first shift trigger to arrive, sets N309, causing pin 8 to go to 0 volts. This positive-going pulse is coupled through capacitor C314 and resets N310, causing pin 5 to go to 0 volts. This changes the back bias on CR305 to 2 volts instead of 20 volts. The second shift trigger now opens CR305 and triggers N318, a 10 microsecond one-shot. The output of this one-shot, pin 8 (Figure 9-15, waveform f.), is the shift request pulse that is sent to the Test-Control Chassis.

3-5.3. Monitor Circuitry

3-5.3.1. The output of N318 is monitored so that if a shift request failure occurs, the Model 74 Data Transmitter will switch over to the redundant circuit in Detector B. The monitor circuit consists of one-shot N314, pulse amplifier N315, one-shot N316, and flip-flop N317. It operates as follows: the shift request pulses from N318 trigger N314, a 500 microsecond one-shot. The output of this one-shot is inverted and has its level changed by N315. Thus, the output of N314 is a 500 microsecond negative-going pulse from 0 volts to -20 volts, and the output of N315 is a positive-going pulse from -10 volts to +12 volts. When pin 4 of N315 is at +12 volts, CR309 conducts, holding pin 6 of N316 at +12 volts. Pin 6 is the positive side of the timing capacitor of one-shot N316. This means that as long as CR309 is conducting, N316 is in its unstable state, and will revert to its stable state at some delay time after CR309 opens.

3-5.3.2. If shift request pulses are not being generated, N314 is not triggered and CR309 stays open. N316 then completes its time delay and pin 5 goes from -20 volts to 0 volts. Flip-flop N317 is then reset; pin 8 going from 0 volts to -20 volts. Pin 8 is connected in series with a relay in the Test-Control Chassis which is tied to -20 volts. When pin 8 of N317 is at 0 volts, the relay is energized and allows the shift request pulse from Detector A to go to the DCC. When pin 8 of N317 goes to -20 volts, the relay drops out and the secondary shift request pulses begin operating.

3-5.3.3. After N317 is reset by N316, it must be returned to its set condition by pushing the RESET pushbutton S503, on the front panel of the Test-Control Chassis. This sends a positive pulse to pin 3 of N317, causing pin 8 to go to 0 volts.

3-6. DETECTOR B CHASSIS, MEC MODEL, 74-3B (See Figures 3-3, 9-7 and 9-8)

3-6.1. The Detector B Chassis converts data from the DCC and inserts it into a Variable Delay Shift Register which drives transmitters 3 and 4. This chassis essentially runs in parallel with Detector A. The data, SOW and EOW outputs from Detector B are inserted into Shift Registers where they are delayed before driving transmitters 3 and 4. This operation is entirely independent of Detector A, which furnishes data, SOW and EOW signals to transmitters 1 and 2. Also included in this chassis is the circuitry for generating the Test ZERO Data Level and the secondary Shift Request pulse.

3-6.2. There are eight outputs from the Detector B Chassis. A SOW pulse is generated for insertion into a shift register when Select and Ready rises; an EOW pulse is inserted at the fall of Select and Ready. Data is sampled and inserted also. Artificial "1"s are generated when the Model 74 is not selected. The data level for an all "0" test pattern is generated in this chassis. (An all "0" has a "1" approximately every 100 microseconds.)

NOTE

Artificial "1"s are identical to data "1"s but are transmitted when the Data Transmitter is deselected. The Model 75 Receiver utilizes these artificial "1" to maintain correct AGC levels and to keep in synchronization with the Data Transmitter.

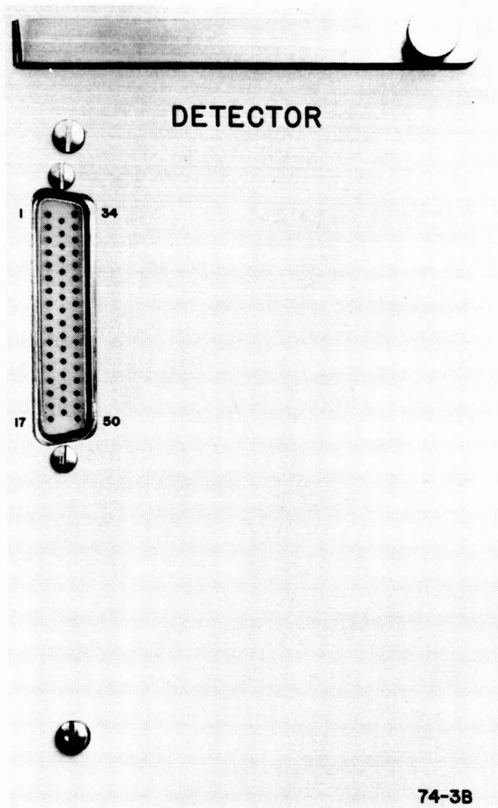


Figure 3-3. Detector B Chassis

3-6.4. Test Select and Ready is generated in this chassis. When in a test mode, the Test Select and Ready so that periodically rises and falls so that SOW, EOW and Selected data can be generated.

NOTE

In normal operation the Data Transmitter transmits to the MEC Model 75 Receiver, which does not use a SOW signal. When loop testing, however, the Data Transmitter transmits to a MEC Model 72 Receiver, which requires an SOW signal.

Test select and ready is also generated in the Detector B Chassis, operating in the Monitor Test, Clock A, or Clock B modes. This is used to raise and lower select and ready periodically for testing purposes.

3-6.5. N310 is a flip-flop used for steering purposes. It is set by the fall of select and ready and reset by the rise of select and ready. Sample trigger pulses enter continuously on pin 8 of TJ301 (Figure 9-15 waveform b.), and are timed to arrive 200 microseconds after the Delay Shift Registers have shifted. When select and ready rises, pin 5 of N310 goes to 0 volts and pin 8 goes to -20 volts. This puts -20 volts on the anode of CR306, while the cathode is at -0.3 volts. The anode of CR308 is at -2 volts while the cathode is at -0.3 volts. Since the sample trigger is less than 20 volts, it does not pass through CR306, but does pass through CR308, triggering N313.

3-6.6. N313 is a 20 microsecond one-shot that is connected in series with the auxiliary winding of the first data core which is, in turn, connected to pin 6 of N312, through CR307. Pin 6 of N312 is at -20 volts when the incoming data (a "1") is at 8 volts. When N313 fires, pin 7 goes from -20 to 0 volts (Figure 9-15 waveform e.). Since pin 6 of N312 is at -20 volts for an incoming "1", current flows through the auxiliary winding, and a "1" is inserted. If the incoming data is a "0", pin 6 of N312 is at 0 volts, and CR307 is back biased. When N313 fires, pin 7 again rises to 0 volts, but current does not flow in the auxiliary winding and a "0" is inserted. When select and ready falls, N310 is set, with pin 5 going to -20 and pin 8 going to 0 volts. The sample trigger now is steered away from N313, since CR308 is back biased and is coupled to N311 through CR306.

3-6.7. N311 is a 20 microsecond one-shot fed into the regular input of the first data core (Figure 9-15 waveform d.). Thus, when select and ready is down, artificial "1"s are generated and the data one-shot is disconnected. With the fall of select and ready, flip-flop N303 is set, causing pin 8 to go to 0 volts. This back biases CR301 by 2 volts. When the first artificial "1" pulse is generated, it fires N304, a 20 microsecond one-shot. This pulse is inserted in the first core of the EOW delay shift register and also resets N303. Pin 8 of N303 now goes to -20 volts, which back biases CR301, keeping it from firing again until select and ready rises and then falls. In this manner only one EOW is generated per word.

3-6.8. N305, N306, and N307 comprise the shift request circuitry. When select and ready falls, flip-flop N306 is set, and pin 5 goes to -20 volts, back biasing CR303 by 20 volts. Thus the shift trigger, which is less than 20 volts, cannot fire N305, a 10 microsecond one-shot. When select and ready rises, flip-flop N307 is reset; pin 8 going to -20 volts and pin 5 going to 0 volts. The next shift trigger that comes in, sets N307, causing pin 8 to go to 0 volts. This positive-going signal is a-c coupled through capacitor C309 and resets N306. Pin 5 of N306 now goes to 0 volts. allowing the next shift trigger to fire N305. The output of N305 is a positive-going pulse going from -20 volts to 0 volts (Figure 9-15 waveform f.). This is the shift request pulse which is fed into the Test-Control Chassis. N306 and N307 thus assure the first shift request trigger does not fire N305. They also delay sending the first shift request pulse for at least one millisecond, after the rise of select and ready. N306 and N307 are called an anti-sliver circuit, the purpose of which is to prevent the generation of a shift request until the first data bit is sampled at least once.

3-6.9. For generating SOW, flip-flop N319, is triggered with the rise of Select and Ready, causing pin 5 to go to 0 volts. On the next core drive trigger N314 is triggered through the AND gate consisting of R357, R358, C331 and CR319. When N314 times out 200 microseconds later, N318, a 20 microsecond one-shot, inserts a "1" into the SOW shift register. The trailing edge of N318 then resets N319 causing pin 5 to return to -20 volts and inhibits N314 from being triggered on the next core drive trigger.

3-6.10. Networks N315 and N316 are used to generate a cyclic Test Select and Ready. These TN's are both one-shots which are cross-connected so that the trailing edge of N315 triggers N316 and vice-versa. Network N316 has a time period of approximately 600 microseconds, and N315 has a period of approximately 100 microseconds. When pin 7 of N316 goes positive, it resets N317, causing pin 5 to go to 0 volts. This 0 volts is then sent to the Test Control Chassis at the rise of Select and Ready. When the Model 74 Data Transmitter is in the Monitor Test, Clock A, or Clock B modes, the output of a counter driven by the shift request pulse is fed into Detector B Chassis. The output of this counter is switched from one collector to the other when going from a "0-1" test pattern. After pin 5 of N316 goes to 0 volts, the next positive-going voltage coming from the counter in Test-Control, sets flip-flop N317, causing pin 5 of N317 to go to 20 volts. The output of pin 5 is fed into Test-Control and is raised to a higher voltage level to simulate the rise and fall of select and ready.

3-6.11. The counter that triggers N317 also supplies the data level in the Test-Control Chassis. If the data pattern is "1-0" and N316 has just completed its time delay, sending the voltage at pin 5 of N316 to 0 volts, the output of the counter fed to Detector B Chassis is taken from the same collector as that fed into the data line. If, in addition, a "1" was just sampled on the data line, a shift request will occur and the counter will reverse its output, causing a negative-going voltage to appear on the test select and ready reset line. The data is sampled 200 microseconds later, and will show a "0" 800 microseconds after sampling. Another shift request will occur. The counter input to the data lines will now show a "1". However, this same "1" caused a positive spike at pin 6 of N317 and set N317. Pin 5 on N317 now becomes negative and select and ready falls. Select and ready will fall before the next sample time; therefore, the last data bit sampled will be a "0", and a "1-0" pattern is created. For a "0-1" pattern, the opposite output of the counter is fed to N317, while the same output is fed to the data line, and a "1" is the last bit sampled. N315 then completes its time delay, triggering N316. When N316 is triggered, N317 is reset, causing select and ready to rise; then the cycle is repeated.

3-6.12. When N317 is reset, the d-c gating input to N320 and N323 is raised. N320 and N323 are 10:1 counters that provide an output pulse when the pulse inputs have been pulsed 10 times. When the pin 6 inputs to N320 and N323 are raised to 0 volts, the counters are inhibited. When N317 is set, the gating inputs to N320 and N323 are lowered and the inhibit function is removed. The trailing edge of N313 then triggers N321, 1 15 microsecond one-shot. This one-shot pulses N320. The output of N320 then pulses N323. This gives a 100:1 countdown. When N323 fires, it triggers N322 and inserts a "1" in the test data word. In this manner a "1" is inserted every 100 milliseconds when in an all "0" test pattern.

3-7. DATA KEYER, MEC MODEL 71-12A (Figures 3-4, 9-9 and 9-10)

3-7.1. The Data Keyer has three signal inputs: SOW, data, and EOW. All of these inputs are positive going pulses of 10 volts amplitude and of approximately 10 microseconds duration. By proper adjustment, the Keyer responds to these pulses by transmitting bursts at a frequency of 2kc for 2 1/2 milliseconds for SOW, 1/2 millisecond for data, and 4 1/2 milliseconds for EOW, respectively. In addition, the Keyer is designed to permit recording of the data and, if desired, to accept the data from a recorder instead of the normal input pulses.

3-7.2. When any of the one-shots, N1201, N1202, or N1203, are triggered, its pin 5 goes from 0 volts to -25 volts. The outputs of these one-shots are "OR" gated, the gate consisting of resistor R1201, and diodes CR1201, CR1202, and CR1203. When one or more of these one-shots are triggered, the grid of V1201A goes to -25 volts, and V1201A is cut off. This allows the magnetic field built up around inductor L1201 to collapse, and the tank circuit of inductor L1201, and capacitors C1202, and C1203 starts ringing. These oscillations are sustained by V1201B, shaped by L1202 and C1204, and are then amplified by V1202A. After amplification, they are fed into V1202B where equal and opposite outputs appear on the plate and cathode. These outputs are fed into V1203, a twin triode, which is operating push-pull. T1201 is used to match the push-pull output to a 600 ohm transmission line. For stabilization and reduction of distortion, a negative feedback circuit, consisting of C1208 and R1217 is utilized. To attenuate the signal for recording purposes, C1209, R1218, and R1219 are used. The frequency of the output is adjusted (normally to 2000 cps) by varying L1201. Connected in parallel with L1202 and C1204 is a resistor used for compensating any deviation of L1202 and C1204 from their stated values. The value of this resistor is determined during testing procedures.

3-7.3. If it is desired to transmit signals that have been recorded, K1201 is energized, switching the input to V1202A from the internal oscillator to pin 9 of P1201 which is connected to the output of a magnetic tape recorder. C1205 and R1208 are utilized as a high pass filter to minimize hum and extraneous noise.

3-7.4. The high voltage Power Supply for the Data Keyer Chassis is contained internally, 120 vac, 60 cycles, entering on pins 39 and 40 of P1201. This passes through T1202 and is rectified and filtered. V1204 and V1205 maintain a voltage reference for the high voltage supply.

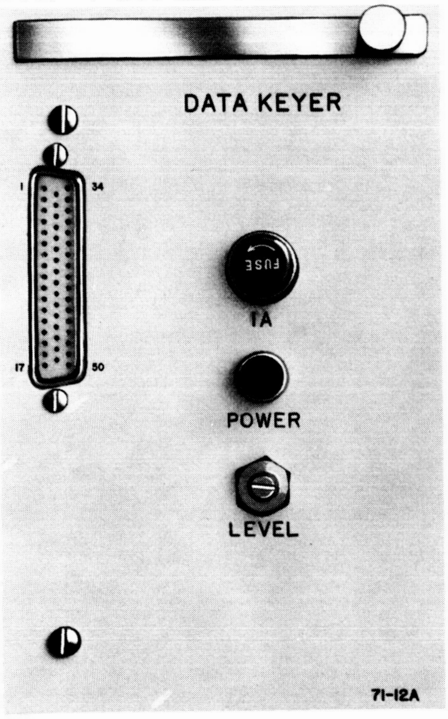


Figure 3-4. Data Keyer Chassis

3-8. VARIABLE DELAY SHIFT REGISTER, MEC MODEL 74-8A and MEC MODEL 74-8B (Figures 3-5, 9-11, and 9-12)

3-8.1. The Variable Delay Shift Register delays data SOW and EOW to transmitters. Network N2, N9 and N5 are blocking oscillators used to shift the magnetic cores used in the Chassis. All three blocking oscillators trigger in parallel when a trigger pulse is applied to pin 1 of P1. Data is shifted in cores M41 through M60 (not in that order). SOW is delayed in M12 through M20 and M22 through M29 (not in that order); EOW is delayed in cores M2 through M11 and M30 through M39 (not in that order).

3-8.2. Data is inserted in the auxiliary winding of M49, artificial "1"s are inserted into the input winding of M49, SOW is inserted in the input winding of M12, and EOW is inserted into the input winding of M2. The output of the last 17 cores in each string is connected to two switches in addition to being run to the input of the next core in the string. The data and EOW strings have three more cores than does the SOW string. Since each core represents one time slot, data pulses and EOW pulses and EOW pusles are delayed three time slots with respect to a SOW pulse. These three time slots allow for the 2.5 microsecond transmission of SOW from akeyer.

3-8.3. The switches used in the chassis are three-pole, 17-position rotary type, with data routed through one pole, SOW routed through the second pole and EOW routed the third pole. The switches are so wired that if a pulse is inserted into the data, SOW and EOW strings simultaneously, the SOW pulse will appear three time slots ahead of data and EOW.

3-8.4. The two switches have their respective stationary contact wired to the output of the same time related core in each string. Since each switch is used to correct one keyer to the Shift Register, the inputs to each keyer may be delayed independently of each other. The rotary contacts of each switch then feed data, SOW and EOW to a keyer, and EOW and data outputs one-shots in the chassis. These one-shots drive neon indicators located on the front panel of each chassis and give a visual indication to the operator that data and EOW are being sent to the keyers.

3-8.5. Since the cores are shifted once every millisecond, the switch position on the front panel indicates a delay time in milliseconds when referenced to each other.

3-8.6. The only difference between the 74-8A and 74-8B registers is the front panel engraving, the 8A reading XMTR #1 three XMTR #2, the 8B reading XMTR #3 and XMTR#4.

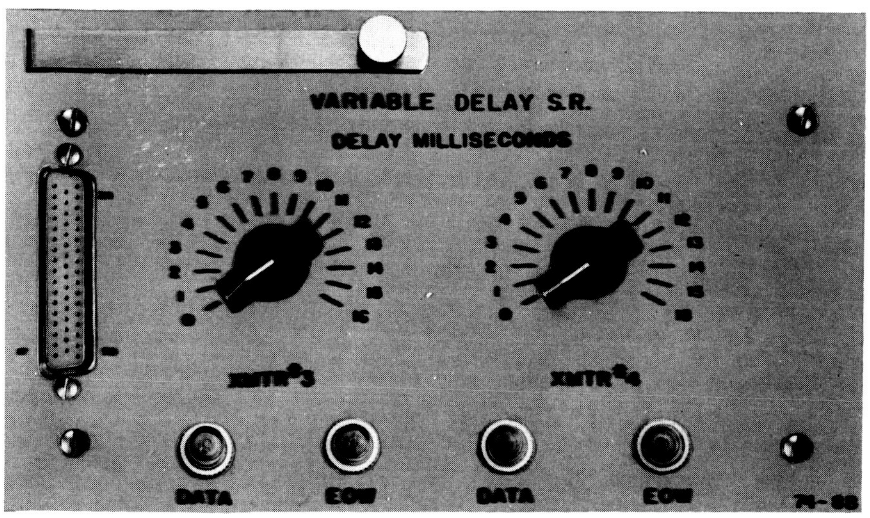


Figure 3-5. Variable Delay Shift Register

3-10. RECORDER CONTROL CHASSIS, MEC MODEL 74-7A (Figures 3-7, 9-16,9-17)

3-10.1. General

3-10.1.1. The function of the Recorder Control Chassis is to select live data from the Impact Predictor (IP) IBM-7090 and Burroughs-General Electric (B-GE) Computers at Cape Canaveral or it will select the playback of recorded data from either or both of these sources from Operational Data Recorder (ODR) 1. The unit will also provide a Control function to select live data from the Goddard Space Flight Center (GSFC) IBM-7090 Computer for transmission to the Mercury Control Center, or to select the playback of this recorded data for transmission to the Mercury Control Center from ODR 2. Therefore, ODR 1 is used for recording and playing back of all high-speed data inputs to the GSFC, whild ODR 2 is used for the recording and playing back of data that originates at GSFC. The controls for the Record and Playback mode of the ODR's are mounted on the Tape Deck of these units. The Recorder Control Chassis provides the selection of data only.

3-10.1.2. INPUT SELECT switch S701 controls the selection of input data from Cape Canaveral to Data Receiver, MEC Model 72, at GSFC. The four positions of the switch are OPERATE, B-GE, IP, and B-GE/IP. The function of each position is discussed in the following paragraphs.

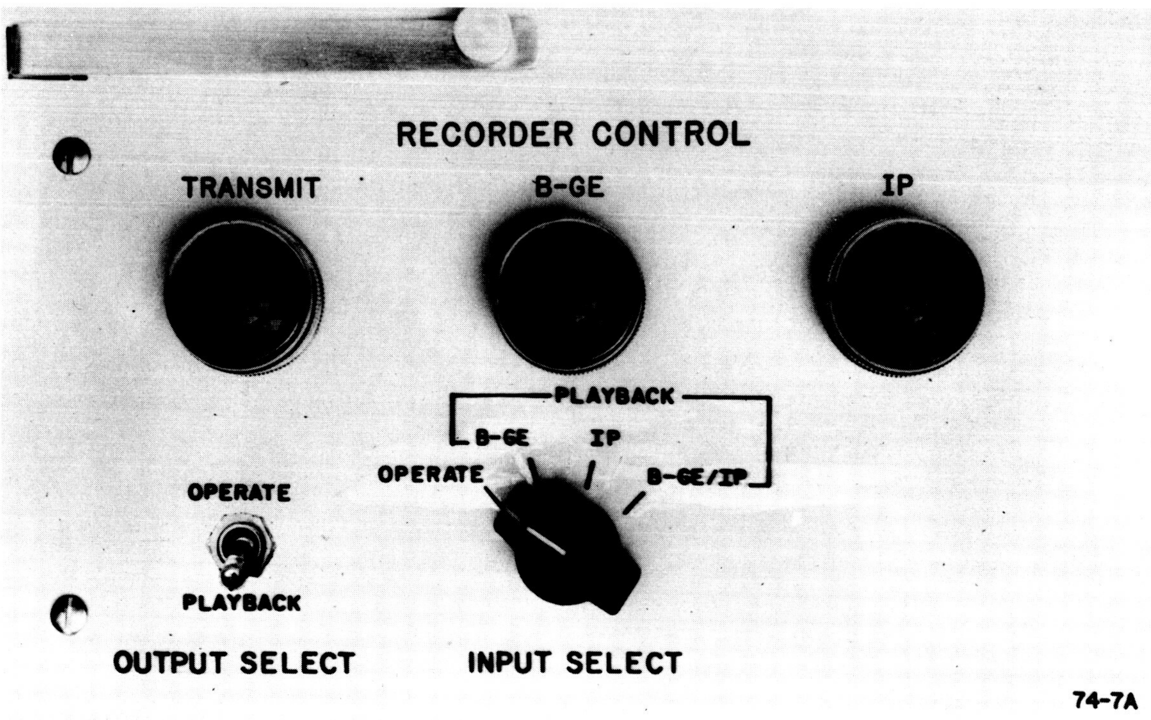


Figure 3-7. Recorder Control Chassis

3-10.1.3. The function of the OUTPUT SELECT switch, S702, is to allow data that is being transmitted by the MEC Model 74 Data Transmitter to Cape Canaveral to be recorded by ODR 2 and played back at some future time. The four inputs of Data Keyers 1 through 4 in the Model 74 Data Transmitter are coupled to the Record inputs of ODR 2. The two positions, OPERATE and PLAYBACK, of OUTPUT SELECT switch S702 are discussed in the following paragraphs.

3-10.2. OPERATE (INPUT SELECT Switch)

When the INPUT SELECT switch is in the OPERATE position, the IP Input lines 1 and 2 and the B-GE Input lines 1 and 2 will be connected, via the normally closed contacts of relays K701 through K704, to the Data Line Amplifier (DLA) inputs 1 through 4, respectively. The DLA inputs 1 through 4 are also connected to the Record inputs 1 through 4 of ODR 1. If ODR 1 is in the Record mode, data from Cape Canaveral (IP and B-GE Computers) will be direct-coupled to the input of the DLA's in the Model 72 Data Receiver. If ODR 1 is in the Record mode, this data will be recorded on magnetic tape.

3-10.3. B-GE (INPUT SELECT Switch)

When the INPUT SELECT switch is in the B-GE position, relays K703 and K704 will be energized, via contact 2 of S701B, if ODR 1 is in the Playback mode. This will allow -20 volts to be coupled through the normally closed set of contacts of K2 and the closed set of contacts of K1 in the ODR to the wiper of S701B. With the switch in the B-GE position, the wiper will be connected to contact 2 of S701B, which will couple -20 volts to pin 3 of K703 and K704. This will likewise energize indicator I702, indicating the INPUT SELECT switch is in the B-GE position, and the Recorder (ODR 1) is in the Playback mode. When K703 and K704 are energized, their normally closed sets of contacts will open, disenabling data on B-GE Input lines 1 and 2 from being coupled to DLA 3 and 4 inputs, respectively. The normally open contacts of K703 and K704 will be closed, coupling the Tape outputs 3 and 4 to DLA 3 and 4 inputs, respectively. The Tape outputs 3 and 4 are the playback of the pre-recorded B-GE Input lines 1 and 2, respectively. When the INPUT SELECT switch is in the B-GE position, it does not affect the incoming IP data; that is, the IP Input lines 1 and 2 are still direct-coupled via the normally closed contacts of K701 and K702 to DLA inputs 1 and 2.

3-10.4. IP (INPUT SELECT Switch)

When the INPUT SELECT switch is in the IP position, and ODR 1 is in the Playback mode, -20 volts will be coupled via K2 and K1 of ODR 1 to the wiper of

S701A. Since the switch is in the IP position, -20 volts will be coupled via this wiper to contact 3 of S701A, which is connected to **pin** 3 of K701 and K702, causing these relays to become energized. It will also cause indicator I703 to light, indicating the switch is in the IP position and ODR 1 is in the Playback mode. The IP data on input lines 1 and 2 will be disconnected from the inputs of DLA 1 and 2. The normally open set of contacts of K701 and K702 will now close, allowing Tape outputs 1 and 2 to be direct-coupled to the DLA 1 and 2 inputs. IP data will now be played back from the magnetic tape to DLA inputs 1 and 2. When the switch is in the IP position, it will not prevent the B-GE Input lines 1 and 2 from being coupled to the input of DLA's 3 and 4, respectively.

3-10.5. B-GE/IP (INPUT SELECT Switch)

When the switch is in the B-GE/IP position, and ODR 1 is in the Playback mode, -20 volts on the wiper of S701A will be coupled to relays K701 and K702 and indicator I703 via contact 4 of S701A. Relays K703 and K704 and indicator I702 will be coupled to -20 volts via contact 4 to the wiper of S701B. All of the relays will be energized, K701 through K704, causing the live data on IP Input lines 1 and 2 and B-GE Input lines 1 and 2 to be disconnected from the inputs of DLA 1 through 4, respectively. The normally open contacts of K701 and K704 will now close, allowing the pre-recorded data of these live inputs to be played back to the inputs of DLA 1 through 4. Both the B-GE and IP indicators will be lit, signifying the inputs to the Model 72 Receiver are from the magnetic tape on ODR 1.

3-10.6. OPERATE (OUTPUT SELECT Switch)

When the OUTPUT SELECT switch, S702, is in the OPERATE position, and ODR 2 is in the Record mode, data that is being transmitted from the Model 70 Data Transmitter will be recorded by ODR 2.

3-10.7. PLAYBACK (OUTPUT SELECT Switch)

When the OUTPUT SELECT switch is in the PLAYBACK position, and ODR 2 is in the Playback mode, -20 volts will be coupled via the closed contacts of K2 and K1 in ODR 2 to the wiper of S702, and via contact 6 of S702 to the TRANSMIT indicator, I701. This voltage will also be coupled from S702 to P701-49, where via rack wiring it will be connected to pin 12 of the relays in Data Keyers 1 through 4, causing these relays to become energized. When the relays in the Data Keyers are energized, the data that is received by the Data Transmitter from the IBM-7090 Computer will not be transmitted by the Data Keyers. Data that is on the magnetic tape of ODR 2 (previously recorded Computer data) will be played back to Data Keyers 1 through 4 so that this data will be transmitted to Cape Canaveral.

CHAPTER IV
OPERATION

With all rack connectors properly connected, and a-c power supplied to the Data Transmitter, the following steps are required to make the unit operative:

a. Place the main power switch SW1, located at the rear of the rack, to the ON position. The red power indicator I1 at the rear of the rack will light.

b. Place power switch S401, on the Power Control Chassis to the ON position.

c. Allow approximately one minute for warm up time.

d. Check all voltages on the Power Control Chassis with a voltmeter. The voltmeter should read between 9.5 and 10.5 in all positions of the VOLTAGE SELECTOR switch S402 (except the OFF position).

e. Turn the MASTER SELECTOR switch S506, on the Test-Control Chassis, to MONITOR TEST. If the MONITOR INDICATOR is on, push the MONITOR RESET button.

f. Select the data pattern desired with switch S507. If the TEST DATA switch is already on the desired pattern, rotate it to another position; then return it to its original position. This will start the select and ready oscillator.

g. Observe the indicator lamps on the Shift Register Chassis. They should now be blinking.

h. Monitor the output of Data Keyer #1, using an oscilloscope with a delayed sweep. Place the oscilloscope ground on pin 7 of the Keyers test jack and place the probe on pin 5 of the test jack. The SOW signal should be a five cycle burst of a 2 kc carrier. The data bits should be 3.1 volts in amplitude, peak to peak, and one cycle of a 2 kc carrier. The EOW signal should be a nine cycle burst of the 2 kc carrier, and should be preceded by the pattern selected on the TEST DATA switch. For example: in a "1-0" pattern, a "O" will precede the EOW. Each data bit fills only one half of a time slot. An all "1"s pattern is one cycle of 2 kc followed by 1/2 millisecond of the base line, this pattern being repeated as often as required.

i. Rotate the TEST DATA switch and observe the output in each data pattern. (The all "0" pattern has a single "1" inserted approximately 75 microseconds after SOW and every 150 microseconds thereafter.)

j. Push the monitor TEST switch, S505. The indicator lamps should come on and the output will remain the same (it is possible for one word to be ruined during switching of the monitor circuit).

k. Observe the output of each data pattern.

l. Push the monitor RESET switch, S503. The monitor indicator lamp will turn off, and the data will remain the same.

m. Repeat steps i through n on each Data Keyer.

The Model 74 Data Transmitter is now ready to operate and will perform as described in previous Chapters. It is strongly urged that this instruction book be thoroughly read and completely understood before operating the equipment.

CHAPTER V

INSTALLATION

5-1. EXTERNAL CONNECTIONS

Provisions should be made to supply the Model 74 Data Transmitter with 120 vac at less than 10 amperes as power input. The Transmitter receives a-c power through J15 at the rear of the rack. Connections between the Transmitter and the DCC are made at J17, and J16 serves as the connector for the telephone voice lines.

5-2. PHYSICAL PLACEMENT

The rack should be installed on a reasonably flat surface, and if it is to be installed near a wall, its rear portion should not be less than three feet from the wall. This enables easy access to the rack through the rear door.

5-3. ADJUSTMENTS AND CABLE FABRICATION

Adjustments and procedures to be executed prior to operating the equipment will be found in CHAPTER IV, OPERATION. Wire size and cable fabrication information will be found in CHAPTER VIII, WIRE LIST.

CHAPTER VI

MAINTENANCE

6-1. CORRECTIVE MAINTENANCE

6-1.1. The first step in corrective maintenance is to become acquainted with the TN networks listed in the Appendix of this manual (Chapter X). In the following procedures, it is assumed that the maintenance technician has done this. It is also assumed that the technician is acquainted with semiconductor devices, their operation and limitations, and procedures for determining when they are not functioning.

6-1.2. The first procedure to be followed when trouble occurs is to check all power supplies by means of the indicator lights and the voltmeter, all of which are located on the Power Control Chassis. If these prove to be operating correctly, check the voltage at each chassis. By referring to the schematics of the individual chassis, the correct pin numbers can be found for each voltage to be checked.

6-1.3. The next general procedure to be followed is that of checking the outputs of each chassis and comparing the output to the input to see if a discrepancy exists. Once the trouble has been isolated to a particular chassis, the technician will find a detailed explanation of each chassis in CHAPTER III, THEORY OF OPERATION.

6-1.4. The Test-Control Chassis should be checked first. The outputs of this chassis are controlled by the tuning forks, driving one-shots and emitter followers. These outputs are fed to the other chassis and should be observed on TJ501. In the monitor test mode, outputs should appear on pins 10, 13, 21, 22, 23, and 24. If any of these are missing, or if they are not greater than 15 volts in amplitude, either TF501, N505, N506, TF502, N508, or N509 are not functioning correctly. If these circuits are all operating correctly, check the Detectors. If the Detectors are functioning correctly, check the Shift Registers, and if these are not at fault, check the Keyers.

6-1.5. By following the block diagram of the system and using the schematics of the chassis (Chapter IX) any trouble should be isolated in a short time.

6-2. PREVENTIVE MAINTENANCE

6-2.1. Check the Data Keyers periodically for proper adjustment. The first adjustment made shall be on the 2kc oscillator. To accomplish this, allow the Keyer to warm up for 30 minutes, then jumper pin 2 of V1201 to -25 volts. By using a dual trace oscilloscope, compare pin 6 of V1202 to pin 23 of TJ501 on the Test-Control Chassis. Since the output of pin 23 of TJ501 has a 1kc repetition rate the output of pin 6 of V1202 must occur twice as often. Adjust L1201 to obtain the proper 2:1 ratio between the two traces on the scope. Then remove the jumper between pin 2 of V1201 and -25 volts.

6-2.2. With the Transmitter in the monitor test mode, place loop test switch ON, choose an all "1"s data pattern, and adjust the time delays of N1201, N1202 and N1203. To do this, observe the output of the Keyer. The data pulse should be one cycle of 2 kc with a minimum of overshoot (0.5 millisecond). Adjust potentiometer R1225 to obtain this result. After R1225 is adjusted, adjust R1226 so that the SOW burst is five cycles of 2kc with a minimum of overshoot (2.5 millisecond), and adjust R1227 for an EOW burst that is nine cycles wide (4.5 millisecond).

6-2.3. While still observing the output, adjust L1202 to produce a narrow sine wave; then adjust R1209 to set the required output level.

6-2.4. Adjust the d-c voltage when necessary by monitoring the voltmeter on the Power Control front panel. All potentiometers for adjusting voltages are located on the front panel of the Power Supplies and are plainly labeled. Adjust each one until the voltmeter reads 10. Adjust the d-c voltages periodically by using a Triplett 630NA VOM or equivalent. Monitor these voltages from the front panel of each Power Supply and adjust them by the potentiometers located on the front panels. Record the reading of the panel meter on the Power Control Chassis in each setting. The panel meter may now be used for day to day voltage checks.

6-2.5. It is strongly urged that this instruction book be thoroughly read and completely understood before operating the equipment.

CHAPTER VII

PARTS LIST

The MEC Model 74 Data Transmitter consists of the following assemblies:

Quantity	Assembly
4	MEC Model 71-12A, Data Keyer
1	MEC Model 74-5A, Test Control
1	MEC Model 74-3A, Detector
1	MEC Model 74-3B, Detector
1	MEC Model 74-8A, Variable Delay Shift Register
1	MEC Model 74-8B, Variable Delay Shift Register
1	MEC Model 74-4A, Power Control
1	MEC Model 74-7A, Recorder Control
2	MEC Model 165-4C, Power Supply
1	Blower
1	MEC Model 74-9A, Four Channel Test Data Keyer

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
12-1				MEC 71-12A	Assembly, Data Keyer	1	
12-2	C1201 C1205 C1209 C1214			Cornell Dubilier PM4S1	Capacitor, Fixed Mylar, .01uf, 400vdc	4	
12-3	C1202 C1203			Cornell Dubilier PM4S2	Cpaacitor, Fixed Mylar, .02uf, 400vdc	2	
12-4	C1204			MIL CM-19B-122K	Capacitor, Fixed Mica, 1200uuf, 500vdc ±10%	1	
12-5	C1206 C1207			MIL CM-19B102K	Capacitor, Fixed Mica, 1000uuf, 500vdc ±10%	2	
12-6	C1208 C1213			Cornell Dubilier PM4P47	Capacitor, Fixed Mylar, .47uf, 400vdc	2	
12-7	C1210			Aerovox AEP88J	Capacitor, Fixed Dual Plug-in, 40-40uf, 450vdc	1	
12-8	C1211			Cornell Dubilier PM4S33	Capacitor, Fixed Mylar, .033uf, 400vdc	1	
12-9	C1212			Cornell Dubilier PM4P22	Capacitor Fixed Mylar, .22uf, 400vdc	1	
12-10	CR1201-CR1204			Transifron T12G or Clevite CTP-503	Diode	4	
12-11	CR1205 CR1210			GE IN1695	Diode	6	
12-12	CR1211			International Rectifier IN1528	Diode, Zener (25V)	1	
12-13	DS1201			Eldema 1CG12-4535	Indicator, Neon to Spec. 21C-3864-7	1	
12-14	F1201			Bussmann AGC	Fuse, 1 Amp	1	
12-15	K1201			Magnecraft 11HPX-59	Relay, 2 Form C	1	
12-16	L1201			UTC HVC-6	Inductor	1	
12-17	L1202			UTC HVC-8	Inductor	1	
12-18	N1201-N1203			MEC TN-51 B	Transistor Network	3	

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
12-19	P1201			Cannon DD-50P	Plug	1	
12-20	R1201			MIL RC20GF105K	Resistor, Fixed Composition, 1M, ±10%, ½W	1	
12-21	R1202 R1212 R1213 R1217 R1218 R1223 R1228			MIL RC20GF104K	Resistor, Fixed Composition, 100K, ±10% ½W	7	
12-22	R1203			MIL RC20GF564K	Resistor, Fixed Composition, 560K, ±10% ½W	1	
12-23	R1204 R1208			MIL RC20GF103K	Resistor, Fixed Composition, 10K, ±10%, ½W	2	
12-24	R1205			MIL RC20GF222K	Resistor, Fixed Composition, 2.2K, ±10%, ½W	1	
12-25	R1206			MIL RC20GF333K	Resistor, Fixed Composition, 33K, ±10%,½W	1	
12-26	R1207			MIL RC20GF472K	Resistor, Fixed Composition, 4.7K, ±10% ½W	1	
12-27	R1209			Allen Bradley JLU-5031 or JAIL040S504UC	Potentiometer, 50K, 2W, Linear Taper	1	
12-28	R1210			MIL RC20GF332K	Resistor, Fixed Composition, 3300 Ohms ±10%, ½W	1	
12-29	R1211			MIL RC20GF224K	Resistor, Fixed Composition, 220K, ±10% ½W	1	
12-30	1214 1216			MIL RC20GF474K	Resister, Fixed Composition, 470K, ±10% ½W	2	
12-31	R1215			MIL RC32GF182K	Resistor, Fixed Composition, 1800 Ohms ±10%, 1W	1	
12-32	R1219			MIL RC20GF223K	Resistor, Fixed Composition, 22K, ±10%, ½W	1	
12-33	R1220			MIL RC42GF511J	Resistor, Fixed Composition, 510Ω, ±5%, 2W	1	
12-34	R1221			Ward Leonard 10X4000	Resistor, Fixed Axiohm, 4K, ±10%, 10W	1	
12-35	R1224			Ward Leonard 5X2000	Resistor, Fixed Axiohm, 2K, ±10%, 5W	1	
12-36	R1225-R1227			Allen Bradley JLU-1041 or JAIL040S104UC	Potentiometer, 100K, 2W, Linear Taper	3	
12-37	T1201			Triad HS-52	Transformer	1	

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCURE-MENT CODE
12-38	T1202			Chicago Std. PHC-55	Transformer	1	
12-39	TJ1201			Cannon DD-505	Connector	1	
12-40	V1201			Comm 12AT7	Tube, Electron	1	
12-41	V1202 V1203			Comm 5963	Tube, Electron	2	
12-42	V1204			Comm OB2	Tube, Electron	1	
12-43	V1205			Comm OA2	Tube, Electron	1	
12-44	XC1210 XK1201 XN1201-XN1203			JAN TS101P01	Socket, Octal, Mica Filled	5	
12-45	XF1201			Bussmann HKP	Fuseholder	1	
12-46	XV1201-XV1203			JAN TS103P01	Socket, Tube 9 Pin Miniature, Mica Filled	3	
12-47	XV1204 XV1205			JAN TS102P01	Socket, Tube, 7 Pin Miniature, Mica Filled	2	
12-48	XDS1201			Eldema 11H-4593	Indicator Holder	1	
12-49				JAN TS103U02	Shield, Tube	3	
12-50				JAN TS102U02	Shield, Tube	2	
12-51				Eldema 11H-4119	LENS, Cap (Red)	1	

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCURE-MENT CODE
5-1				MEC 74-5A	ASSEMBLY, TEST CONTROL	1	
5-2	C501, C503			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000μμf 500 vdc ±10%	2	
5-3	C506,			MIL CM-19B-561K	CAPACITOR, Fixed Mica, 560μμf 500 vdc ±10%	1	
5-4	C502, C504			Cornell Dubilier PM4P1	CAPACITOR, Fixed Mylar, .1μf 400 vdc	2	
5-5	C505, C516			Cornell Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02μf 400 vdc	2	
5-6	C507			MIL CM-19B-681K	CAPACITOR, Fixed Mica, 680μμf 500 vdc ±10%	1	
5-7	C510, C512			Fansteel F110-1	CAPACITOR, (Blu-Cap) 10μf 25 vdc	2	
5-8	C511, C513 C514			Fansteel F308-1	CAPACITOR, (Blu-Cap) 100μf 30 vdc	3	
5-9	CR501, CR502, CR512			G.E. IN1692	DIODE	3	
5-10	CR503, CR504, CR511			Transitron T12G or Clevite CTP-503	DIODE	3	
5-11	CR505 CR510			International Rectifier IN1525	DIODE, Zener (1Z15)	2	
5-12	CR506			International Rectifier IN1523	DIODE, Zener (1Z10)	1	
5-13	CR507, CR508			Pacific Semi-Conductor IN703	DIODE, Zener	2	
5-14	CR509			Motorola 10M10Z	DIODE, Zener	1	
5-15	DS501 DS502			MEC 16-102	INDICATOR	2	
5-16	I501 I502			Dialight Corp. 656	LAMP, Incandescent, Candelabra, Base, 125V Clear	2	
5-17	K501			C.P. Clare RP-4461-G28	RELAY, Type J, 4 Form C (Type 2)	1	
5-18	K502			MEC RY-11	RELAY	1	
5-19	N501, N510-N512			MEC TN-58	TRANSISTOR NETWORK	4	
5-20	N502			MEC TN-57	TRANSISTOR NETWORK	1	
5-21	N503, N504 N506, N509			MEC TN-111	TRANSISTOR NETWORK	4	
5-22	N505, N508			MEC TN-157	TRANSISTOR NETWORK	2	
5-23	N507			MEC TN-90B	TRANSISTOR NETWORK	1	
5-24	P501			Cannon DD-50P	PLUG	1	
5-25	R525			MIL RC20GF302J	RESISTOR, Fixed composition, 3K ±5% 1/2W	1	
5-26	R501, R510			MIL RC20GF153K	RESISTOR, Fixed composition, 15K ±10% 1/2W	2	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
5-27	R502, , R518 R526, R528			MIL RC20GF103K	RESISTOR, Fixed composition, 10K ±10% 1/2W	5	
5-28	R503, R511 R529			MIL RC20GF332K	RESISTOR, Fixed composition, 3.3K ±10% 1/2W	3	
5-29	R530, R531			MIL RC42GF910J	RESISTOR, Fixed composition, 91Ω ±5% 2W	2	
5-30	R505, R506 R508, R523-R524			MIL RC20GF104K	RESISTOR, Fixed composition, 100K ±10% 1/2W	5	
5-31	R507, R520			MIL RC20GF273K	RESISTOR, Fixed composition, 27K ±10% 1/2W	2	
5-32	R514, R519			MIL RC20GF391K	RESISTOR, Fixed composition, 390Ω ±10% 1/2W	2	
5-33	R515			MIL RC20GF102K	RESISTOR, Fixed composition, 1K ±10% 1/2W	1	
5-34	R516, R517			MIL RC20GF472K	RESISTOR, Fixed composition, 4.7K ±10% 1/2W	2	
5-35	S501-S503 S505			Micro 2PB11	SWITCH, Pushbutton	4	
5-36	S504			Carling 2GL63-73	SWITCH, Toggle, DPDT	1	
5-37	S507, S508			Centralab PA-2007	SWITCH, Rotary	2	
5-38	TF501 TF502			Philamon J1000K-N4085	TUNING FORK	2	
5-39	TJ501			Cannon DD-50S	CONNECTOR	1	
5-40	XI501 XI502			Dialight Corp. 514001-111	INDICATOR HOLDER	2	
5-41	XK501			Eby 9759-5	SOCKET, Relay, 14 Pin	1	
5-42	XN501-XN512 XK502			JAN TS101P01	SOCKET, Octal, Mica filled	13	
5-43				Whitso K-105	KNOB	3	
5-44	S509			Cutler Hammer 8363K7	SWITCH, Toggle, DPDT	1	

ASSEMBLY 74-3A REV #4

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
3-1				MEC 74-3A	ASSEMBLY, DETECTOR "A"			
3-2	C335			MIL CM-19B-471K	CAPACITOR, Fixed mica, 470mmfd, 500vdc, 10%	1		
3-3	C330			Fansteel F308-1	CAPACITOR (Blu-Cap), 100mfd, 30vdc	1		
3-4	C331			Fansteel F110-1	CAPACITOR (Blu-Cap), 10mfd, 25vdc	1		
3-5	C333			Cornell-Dubilier PM4S22	CAPACITOR, Fixed Mylar, .022mfd, 400vdc	1		
3-6	C301, C306 C334			MIL CM-19B-331K	CAPACITOR, Fixed Mica, 330mmfd, 500vdc, 10%	3		
3-7	C302, C304 C307, C312 C314, C315 C317, C318 C326, C327			MIL CM-19B-561K	CAPACITOR, Fixed Mica, 560mmfd, 500vdc, 10%	10		
3-8	C305			MIL CM-19B-182K	CAPACITOR, Fixed Mica, 1800mmfd, 500vdc, 10%	1		
3-9	C309, C311 C322			MIL CM-19B-152K	CAPACITOR, Fixed mica, 1500mmfd, 500vdc, 10%	3		

4A-6-62

3-10	C310 C323			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000mmfd, 500vdc, 10%	2		
3-11	C321 C328			MIL CM-19B-681K	CAPACITOR, Fixed Mica, 680mmfd, 500vdc, 10%	2		
3-12	C324			Cornell-Dubilier PM4S5	CAPACITOR, Fixed Mylar, .05mfd, 400vdc	1		
3-13	C325			G.E. 29F519-G4	CAPACITOR, Tantalytic, 1mfd, 100vdc	1		
3-14	C329			G.E. 29F585-G4	CAPACITOR, Tantalytic, .05mfd, 75vdc	1		
3-15	C303, C308 C313, C316 C320			MIL CM-19B-221K	CAPACITOR, Fixed Mica, 220mmfd, 500vdc, 10%	5		
3-16	C332			MIL CM-19B-222K	CAPACITOR, Fixed Mica, 2200mmfd, 500vdc, 10%	1		
3-17	CR301-CR308 CR310-CR312 CR314-CR320 CR323 CR324			CTP-503	SEMI-CONDUCTOR DEVICE, DIODE	20		

ASSEMBLY 74-3A **REV** #4

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
3-18	CR309			1N1692	SEMI-CONDUCTOR DEVICE, DIODE	1	
3-19	CR313 CR321 CR322			1N703	SEMI-CONDUCTOR DEVICE, DIODE	3	
3-20	N301, N315 N319			MEC TN58	SEMI-CONDUCTOR DEVICE SET	3	
3-21	N302 N306			MEC TN57	SEMI-CONDUCTOR DEVICE SET	2	
3-22	N303, N307 N309-N311 N320			MEC TN90B	SEMI-CONDUCTOR DEVICE SET	6	
3-23	N304, N305 N308, N316			MEC TN111	SEMI-CONDUCTOR DEVICE SET	4	
3-24	N312-N314			MEC TN138B	SEMI-CONDUCTOR DEVICE SET	3	
3-25	N317			MEC TN79	SEMI-CONDUCTOR DEVICE SET	1	
3-26	N318, N321 N322			MEC TN138	SEMI-CONDUCTOR DEVICE SET	3	
3-27	P301			MEC 27-101	PLUG, Male, 50 Pin Contact, 5 Amp Rating	1	
3-28	R351			MIL RC20GF162J	RESISTOR, Fixed Composition, 1.6K, ±5%, 1/2W	1	
3-29	R301, R302 R341, R342 R303, R343			MIL RC20GF102K	RESISTOR, Fixed Composition, 1K, ±10%, 1/2W	6	
3-30	R304 R344			MIL RC20GF183K	RESISTOR, Fixed Composition, 18K, ±10%, 1/2W	2	
3-31	R308, R309 R316, R321 R323, R326 R328, R330 R335, R339 R340, R349			MIL RC20GF103K	RESISTOR, Fixed Composition, 10K, ±10%, 1/2W	12	
3-32	R306, R312 R325, R336			MIL RC20GF153K	RESISTOR, Fixed Composition, 15K, ±10%, 1/2W	4	
3-33	R307, R313 R314			MIL RC20GF473K	RESISTOR, Fixed Composition, 47K, ±10%, 1/2W	3	
3-34	R305, R310 R317, R318 R322, R327 R331, R332			MIL RC20GF332K	RESISTOR, Fixed Composition, 3.3K, ±10%, 1/2W	8	
3-35	R311, R319 R320, R324 R329, R333 R334			MIL RC20GF333K	RESISTOR, Fixed Composition, 33K, ±10%, 1/2W	7	

ASSEMBLY 74-3A **REV** #4

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
3-36	R350			MIL RC20GF222K	RESISTOR, Fixed Composition, 2.2K, ±10%, 1/2W	1	
3-37	R315, R337 R346			MIL RC20GF472K	RESISTOR, Fixed Composition, 4.7K, ±10%, 1/2W	3	
3-38	R338			MIL RC42GF102K	RESISTOR, Fixed Composition, 1K, ±10%, 2W	1	
3-39	R345			MIL RC20GF152K	RESISTOR, Fixed Composition, 1.5K, ±10%, 1/2W	1	
3-40	R347			MIL RC20GF104K	RESISTOR, Fixed Composition, 100K, ±10%, 1/2W	1	
3-41	R348			MIL RC20GF751J	RESISTOR, Fixed Composition, 750 Ohms, ±5%, 1/2W	1	
3-42	R351			MIL RC20GF223K	RESISTOR, Fixed Composition, 22K, ±10%, 1/2W	1	
3-43	TJ301			Cannon DD50S	CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating	1	
3-44	XN301 - XN322			JAN TS101P01	SOCKET, Tube, Octal	22	
3-45	Spare			JAN TS101P01	SOCKET, Tube, Octal	1	
3-1				MEC 74-3B	ASSEMBLY, DETECTOR "B"		
3-2	C340			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000mmfd, 500vdc, 10%	1	
3-3	C329			Cornell-Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02mfd, 400vdc	1	
3-4	C330			MIL CM-19B-272K	CAPACITOR, Fixed Mica, 2700mmfd, 500vdc, 10%	1	
3-5	C324, C327 C328			MIL CM-19B-471K	CAPACITOR, Fixed Mica, 470mmfd, 500vdc, 10%	3	
3-6	C301-C303 C308, C309 C312, C314 C317			MIL CM-19B-561K	CAPACITOR, Fixed Mica, 560mmfd, 500vdc, 10%	8	
3-7	C305, C318 C319, C333			MIL CM-19B-152K	CAPACITOR, Fixed Mica, 1500mmfd, 500vdc, 10%	4	
3-8	C306 C332			MIL CM-19B-681K	CAPACITOR, Fixed Mica, 680mmfd, 500vdc, 10%	2	
3-9	C311 C331			MIL CM-19B-331K	CAPACITOR, Fixed Mica, 330mmfd, 500vdc, 10%	2	
3-10	C313			G.E. 29F519-G4	CAPACITOR, Tantalytic, 1mfd, 100vdc	1	

ASSEMBLY 74-3B REV #7

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
3-11	C320 C325			Fansteel F110-1	CAPACITOR (Blu-Cap), 10mfd, 25vdc	2	
3-12	C321 C326			Fansteel F308-1	CAPACITOR (Blu-Cap), 100mfd, 30vdc	2	
3-13	C304, C307 C310, C315 C316			MIL CM-19B-221K	CAPACITOR, Fixed Mica, 220mmfd, 500vdc, 10%	5	
3-14	CR301- CR304 CR306- CR315 CR318 CR319			CTP-503	SEMI-CONDUCTOR DEVICE, DIODE	16	
3-15	CR305 CR316 CR317			1N703	SEMI-CONDUCTOR DEVICE, DIODE	3	
3-16	N301 N312			MEC TN58	SEMI-CONDUCTOR DEVICE SET	2	
3-17	N302 N308			MEC TN57	SEMI-CONDUCTOR DEVICE SET	2	
3-18	N303, N306 N307, N310 N317, N319			MEC TN90B	SEMI-CONDUCTOR DEVICE SET	6	
3-19	N304, N309 N311			MEC TN111	SEMI-CONDUCTOR DEVICE SET	3	
3-20	N305, N314 N318, N320 N321			MEC TN138	SEMI-CONDUCTOR DEVICE SET	5	
3-21	N313, N315 N316			MEC TN138B	SEMI-CONDUCTOR DEVICE SET	3	
3-22	N320 N323			MEC TN200	SEMI-CONDUCTOR DEVICE SET	2	
3-23	P301			MEC 27-101	PLUG, Male, 50 Pin Contact, 5 Amp Rating	1	
3-24	R359			MIL RC20GF162J	RESISTOR, Fixed Composition, 1.6K, ±5%, 1/2W	1	
3-25	R357			MIL RC20GF222K	RESISTOR, Fixed Composition, 2.2K, ±10%, 1/2W	1	
3-26	R345			MIL RC20GF123K	RESISTOR, Fixed Composition, 12K, ±10%, 1/2W	1	
3-27	R358			MIL RC20GF223K	RESISTOR, Fixed Composition, 22K, ±10%, 1/2W	1	
3-28	R301, R303 R330, R332 R346, R347			MIL RC20GF102K	RESISTOR, Fixed Composition, 1K, ±10%, 1/2W	6	

ASSEMBLY 74-3B REV #7

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1	2	3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
3-29	R304 R333			MIL RC20GF183K			RESISTOR, Fixed Composition, 18K, ±10%, 1/2W	2		
3-30	R305, R308 R310, R312 R315, R318 R323, R328 R339, R348			MIL RC20GF103K			RESISTOR, Fixed Composition, 10K, ±10%, 1/2W	10		
3-31	R306, R319 R344, R356			MIL RC20GF153K			RESISTOR, Fixed Composition, 15K, ±10%, 1/2W	4		
3-32	R307, R320 R321			MIL RC20GF473K			RESISTOR, Fixed Composition, 47K, ±10%, 1/2W	3		
3-33	R309, R314 R317, R325 R327, R342			MIL RC20GF332K			RESISTOR, Fixed Composition, 3.3K, ±10%, 1/2W	6		
3-34	R311, R313 R316, R324 R326, R340 R343			MIL RC20GF333K			RESISTOR, Fixed Composition, 33K, ±10%, 1/2W	7		
3-35	R322 R329			MIL RC20GF472K			RESISTOR, Fixed Composition, 4.7K, ±10%, 1/2W	2		
3-36	R334			MIL RC20GF152K			RESISTOR, Fixed Composition, 1.5K, ±10%, 1/2W	1		
3-37	R335			MIL RC20GF751K			RESISTOR, Fixed Composition, 750 Ohms, ±10%, 1/2W	1		

4A-6-62

3-38	R338			MIL RC20GF823K			RESISTOR, Fixed Composition, 82K, ±10%, 1/2W	1		
3-39	R341			MIL RC20GF912J			RESISTOR, Fixed Composition, 9100 Ohms, ±5%, 1/2W	1		
3-40	TJ301			Cannon DD-50S			CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating	1		
3-41	XN301 - XN323			JAN TS101P01			SOCKET, Octal	23		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-1				MEC 74-8A	ASSEMBLY, VARIABLE DELAY SHIFT REGISTER			
8-2	C1, C5 C6			Fansteel F110-1	CAPACITOR (Blu-Cap), 10mfd, 25vdc	3		
8-3	C2-C4			Fansteel F308-1	CAPACITOR (Blu-Cap), 100mfd, 30vdc	3		
8-4	C7, C8			Cornell-Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02mfd, 400vdc	2		
8-5	CR1			1N703	SEMI-CONDUCTOR DEVICE, DIODE, Zener	1		
8-6	DS1-DS4			MEC 16-102	LAMP, Neon	4		
8-7	M1, M21 M40			MEC MN13	CORE, Magnetic	3		
8-8	M2-M20 M22-M39 M41-M60			MEC 26-101	CORE, Magnetic	57		
8-9	N2, N4 N5			MEC TN130B	SEMI-CONDUCTOR DEVICE SET	3		
8-10	N1, N3 N6, N7			MEC TN51	SEMI-CONDUCTOR DEVICE SET	4		
8-11	P1			MEC 27-101	PLUG, Male, 50 Pin Contact, 5 Amp Rating	1		
8-12	R1, R2 R5			MIL RC20GF152K	RESISTOR, Fixed Composition, 1.5K, ±10%, 1/2W	3		
8-13	R3, R4			MIL RC42GF27GK	RESISTOR, Fixed Composition, 2.7 Ohm, ±10%, 2W	2		
8-14	R6-R8			MIL RC20GF103K	RESISTOR, Fixed Composition, 10K, ±10%, 1/2W	3		
8-15	R9			MIL RC20GF472K	RESISTOR, Fixed Composition, 4.7K, ±10%, 1/2W	1		
8-16	S1, S2			Oak 399655MF	SWITCH, Rotary	2		
8-17	TJ1			Cannon DD-50S	CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating	1		
8-18	XM1-XM60			JAN TS103P02	SOCKET, Tube, 9 Pin	60		
8-19	XN1-XN7			JAN TS101P01	SOCKET, Octal	7		
8-20				Whitso K-105	KNOB	2		

4A-6-62

Date 7/3/62

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-1				MEC 74-8B	ASSEMBLY, VARIABLE DELAY SHIFT REGISTER			
8-2	C1, C5 C6			Fansteel F110-1	CAPACITOR, (Blu-Cap), 10mfd, 25vdc	3		
8-3	C2-C4			Fansteel F308-1	CAPACITOR (Blu-Cap), 100mfd, 30vdc	3		
8-4	C7, C8			Cornell-Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02mfd, 400vdc	2		
8-5	CR1			1N703	SEMI-CONDUCTOR DEVICE, DIODE, Zener	1		
8-6	DS1-DS4			MEC 16-102	LAMP, Neon	4		
8-7	M1, M21 M40			MEC MN13	CORE, Magnetic	3		
8-8	M2-M20 M22-M39 M41-M60			MEC 26-101	CORE, Magnetic	57		
8-9	N2, N4 N5			MEC TN130B	SEMI-CONDUCTOR DEVICE SET	3		
8-10	N1, N3 N6, N7			MEC TN51	SEMI-CONDUCTOR DEVICE SET	4		
8-11	P1			MEC 27-101	PLUG, Male, 50 Pin Contact, 5 Amp Rating	1		
8-12	R1, R2 R5			MIL RC20GF152K	RESISTOR, Fixed Composition, 1.5K, ±10%, 1/2W	3		
8-13	R3, R4			MIL RC42GF27GK	RESISTOR, Fixed Composition, 2.7 Ohm, ±10%, 2W	2		
8-14	R6-R8			MIL RC20GF103K	RESISTOR, Fixed Composition, 10K, ±10%, 1/2W	3		
8-15	R9			MIL RC20GF472K	RESISTOR, Fixed Composition, 4.7K, ±10%, 1/2W	1		
8-16	S1, S2			Oak 399655MF	SWITCH, Rotary	2		
8-17	TJ1			Cannon DC-50S	CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating	1		
8-18	XM1-XM60			JAN TS103P02	SOCKET, Tube, 9 Pin	60		
8-19	XN1-XN7			JAN TS101P01	SOCKET, Octal	7		
8-20				Whitso K-105	KNOB	2		

4A-6 62

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
4-1				MEC 74-4A	Assembly Power Control	1	
4-2	CR 401- CR 405			GE. IN 1695	Diode	5	
4-3	CR 406 CR 407			GE. IN 1692	Diode	2	
4-4	DS 401- DS 405			Eldema 1CG12-4535	Lamp, Neon To Spec. 21C-3864-7	5	
4-5	I401- I402			Eldema IGF5-4976	Lamp, Incandescent (Red)	2	
4-6	MU 401			Beede E-25	Meter, 102 Ma (Scale 0-12) Horizontal Mounting	1	
4-7	P 401			Cannon DD-50P	Plug	1	
4-8	R 401			Mil RC20GF393K	Resistor, Fixed Composition, 39K, ± 10% 1/2 W	1	
4-9	R402			I.R.C. DCC	Resistor, Precision, 54K ± 1% 1/2 W	1	
4-10	R403			I.R.C. DCC	Resistor, Precision, 12K, ± 1%, 1/2W	1	
4-11	R 404			I.R.C. DCC	Resistor, Precision, 20K, ± 1%, 1/2 W	1	
4-12	R405			I.R.C DCC	Resistor, Precision, 85K, ± 1% 1/2 W	1	
4-13	R406			I.R.C. DCC	Resistor, Precision, 250K, ± 1%, 1/2 W	1	
4-14	R407-			Mil RC20GF104K	Resistor, Fixed Composition, 100K, ±, 10% 1/2 W	8	
4-15	R415 R416			Ward Leonard 10F100	Resistor, Fixed Wire Wound 100Ω, 10w	2	
4-16	R417 R418			Mil RC32GF391K	Resistor, Fixed Composition, 390Ω, ± 10% 1 W	2	
4-17	S401			Cutler Hammer ST52N	Switch, Toggle, DPDT	1	
4-18	S402			OAK 399655-MF	Switch, Rotary	1	
4-19	XDS 401- XDS 405			Eldema 11H-4593	Indicator Holder	5	
4-20				Whitso K-105	Knob	1	
4-21				Eldema 11H-4110	Lens Cap, (Translucent)	1	
4-22				Eldema 11H-4119	Lens Cap, (Red)	4	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
4-1				MEC 165-4C	ASSEMBLY, POWER SUPPLY	1	
4-2	C401 C402 C421-C423			Mallory 20-71937	CAPACITOR, Computer Grade, 4000µf 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	5	
4-3	C403 C425 C443 C444			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01µf 400 vdc	4	
4-4	C424			Cornell Dubilier PM4P1	CAPACITOR, Fixed, Mylar, .1µf 400 vdc	1	
4-5	C404 C426			Fansteel F308-1	CAPACITOR, Blu-cap, 100µf 30 vdc	2	
4-6	C441 C442			Mallory 20-71855	CAPACITOR, Computer Grade, 2000µf 100 vdc, 2-1/16 x 4-1/2 Alum. can with acetate sleeve.	2	
4-7	C445			Fansteel F316-1	CAPACITOR, Blu-cap, 30µf 100 vdc	1	
4-8	CR401 CR421			G. E. 4JA211AB1AC2	RECTIFIER	3	
4-9	CR402 CR422			International Rectifier IN1519	DIODE, Zener (1Z4.7)	2	
4-10	CR442			International Rectifier IN1524	DIODE, Zener (1Z12)	1	
4-11	F401 F403			Bussmann AGC	FUSE, 1 Amp	2	
4-12	F402			Bussmann AGC	FUSE, 3 Amp	1	
4-13	F404			Bussmann MDX	FUSE, Fusetron, Slo-Blow, 3 Amp.	1	
4-14	P401			Cannon DD-50P	PLUG	1	
4-15	Q423 Q442			Delco 2N553	TRANSISTOR, (Mount with Parts #100 & #101)	2	
4-16	Q401 Q421 Q441 Q422			Delco 2N443	TRANSISTOR, (Lug type Leads)	4	
4-17	Q402 Q403 Q424 Q443			G. E. 2N525	TRANSISTOR	4	
4-18	Q404 Q425 Q444			Sylvania 2N377A	TRANSISTOR	3	
4-19	R401, R402 R421A R421B R441 R442			Ward Leonard 5X1	RESISTOR, Axiohm, 1Ω 5W	6	
4-20	R403 R443			Ward Leonard 5X2	RESISTOR, Axiohm, 2Ω 5W	2	
4-21	R404 R425 R444			MIL RC42GF102K	RESISTOR, Fixed composition, 1K ±10% 2W	3	

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCURE-MENT CODE
4-22	R405			MIL RC42GF151K	RESISTOR, Fixed composition, 150Ω ±10% 2W	1	
4-23	R406			MIL RC20GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1/2W	1	
4-24	R407 R428 R447			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	3	
4-25	R408			MIL RC20GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1/2W	1	
4-26	R409 R430 R449			MIL RC20GF822K	RESISTOR, Fixed composition, 8.2K ±10% 1/2W	3	
4-27	R410 R431 R450			MIL RC20GF621J	RESISTOR, Fixed composition, 620Ω ±5% 1/2W	3	
4-28	R411 R432			MIL RC20GF472K	RESISTOR, Fixed composition, 4.7K ±10% 1/2W	2	
4-29	R412			MIL RC32GF121K	RESISTOR, Fixed composition, 120Ω ±10% 1W	1	
4-30	R414 R435			Chicago Tel. RA20LASB250A	POTENTIOMETER, 25Ω 2W	2	
4-31	R415			MIL RC32GF820J	RESISTOR, Fixed composition, 82Ω ±5% 1W	1	
4-32	R413			MIL RC42GF131J	RESISTOR, Fixed composition, 130Ω ±5% 2W	1	
4-33	R422			Ward Leonard 10F1	RESISTOR, Fixed, Wire wound, 1Ω 10W	1	
4-34	R423 R424			Ward Leonard 10F2	RESISTOR, Fixed, Wire wound, 2Ω 10W	2	
4-35	R426 R437			Ward Leonard 10F150	RESISTOR, Fixed, Wire wound, 150Ω 10W	2	
4-36	R427 R446			MIL RC32GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1W	2	
4-37	R429 R448			MIL RC32GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1W	2	
4-38	R433 R416			MIL RC42GF271K	RESISTOR, Fixed composition, 270Ω ±10% 2W	2	
4-39	R436			MIL RC32GF510J	RESISTOR, Fixed composition, 51Ω ±5% 1W	1	
4-40	R434			MIL RC42GF181J	RESISTOR, Fixed composition, 180Ω ±5% 2W	1	
4-41	R451			MIL RC42GF302J	RESISTOR, Fixed composition, 3K ±5% 2W	1	
4-42	R453			Allen Bradley JLU-1011 or JA1L040S101UC	POTENTIOMETER, 100Ω 2W, Linear Taper	1	
4-43	R454			MIL RC42GF272J	RESISTOR, Fixed composition, 2.7K ±5% 2W	1	
4-44	R455			Ward Leonard 5X500	RESISTOR, Fixed, Axiohm, 500Ω 5W	1	
4-45	R452			MIL RC32GF561J	RESISTOR, Fixed composition, 560Ω ±5% 1W	1	
4-46	R445			Ward Leonard 10F250	RESISTOR, Fixed, Wire wound, 250Ω 10W	1	
4-47	T401			TTI 5486	TRANSFORMER	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
4-48	TJ401-TJ404			H.H. Smith 221	JACK, Midget Banana (Black)	4	
4-49	XF401-XF404			Bussmann HKP	FUSEHOLDER	4	
7-1				MEC 74-7A	ASSEMBLY, RECORDER CONTROL	1	
7-2	I701-I703			Dialight 656	LAMP Incandescent, 24V, Candelabra Base	3	
7-3	K701-K704			C.P. Clare RP4461-G28	RELAY (4 Form C)	4	
7-4	P701			Cannon DD-50P	PLUG Male, 50 Pin Contact, 5 Amp Rating	1	
7-5	S701			Centralab PA-2011	SWITCH Rotary, Ceramic	1	
7-6	XI701-XI703			Dialight 514001-113	INDICATOR HOLDER	3	
7-7	XK701-XK704			Eby 9759-5	SOCKET 14 Pin Miniature	4	
7-8				Whitso [illegible]-105	KNOB	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
1				McLean 2EB508C	ASSEMBLY, BLOWER	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
9-1				MEC 74-9A	ASSEMBLY, 4 CHANNEL TEST DATA KEYER			
9-2	C1			Cornell-Dubilier PM4P1	CAPACITOR, Fixed Mylar, .1mfd, 400vdc MEC SPN C-03-06	1		
9-3	C2			Cornell-Dubilier PM4S1	CAPACITOR, Fixed Mylar, .01mfd, 400vdc MEC SPN C-03-01	1		
9-4	C3			Mallory	CAPACITOR, Computer Grade, Style #4, 3000mfd, 75vdc (in 2-1/16 Dia. x 4-1/2 Acetate Insulating Sleeve) MEC SPN C-06-07	1		
9-5	CR1-CR4			IN1692	SEMI-CONDUCTOR DEVICE, DIODE MEC SPN D-01-06	4		
9-6	CR5			IN2984B	SEMI-CONDUCTOR DEVICE, DIODE, Zener, 20V (With Insulated Mounting Hardware) MEC SPN D-01-73	1		
9-7	CR6			IN2976B	SEMI-CONDUCTOR DEVICE, DIODE, Zener, 12V (With Insulated Mounting Hardware) MEC SPN D-01-74	1		
9-8	F1			Buss AGC	FUSE, 1 Amp MEC SPN F-01-11	1		
9-9	I1-I4			Eldema 1CF3-6356	LAMP, Incandescent (Milky Lens) MEC SPN L-01-04	4		
9-10	I5			G.E. S-6	LAMP, Incandescent, Candelabra Screw Base, 110V, Clear MEC SPN L-01-11	1		
9-11	J21			MIL MS3102A-18-11P MS3106B-18-11S MS3057-10	CONNECTOR, Receptacle, with Mating Connector and Cable Clamp MEC SPN C-11-82 MEC SPN C-11-83 MEC SPN C-11-117	1		
9-12	J22			MIL MS3102A-18-11S MS3106B-18-11P MS3057-10	CONNECTOR, Receptacle with Mating Connector and Cable Clamp MEC SPN C-11-83 MEC SPN C-11-82 MEC SPN C-11-117	1		
9-13	J23			MIL MS3102A-22-14P MS3106B-22-14S MS3057-12	CONNECTOR, Receptacle with Mating Connector and Cable Clamp MEC SPN C-11-140 MEC SPN C-11-151 MEC SPN C-11-45	1		
9-14	J24			MIL MS3102A-22-14S MS3106B-22-14P MS3057-12	CONNECTOR, Receptacle with Mating Connector and Cable Clamp MEC SPN C-11-151 MEC SPN C-11-140 MEC SPN C-11-45	1		
9-15	L1			United Transformer Corp. HVC-6	INDUCTOR MEC SPN I-01-01	1		
9-16	N1			MEC TN901	SEMI-CONDUCTOR DEVICE SET	1		

4A-6 59

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
9-17	N2			MEC TN506B	SEMI-CONDUCTOR DEVICE SET	1	
9-18	N3			MEC TN432	SEMI-CONDUCTOR DEVICE SET	1	
9-19	N4, N5			MEC TN4058	SEMI-CONDUCTOR DEVICE SET	2	
9-20	R1			Allen Bradley Type G	POTENTIOMETER, 5K, 1/2W MEC SPN P-02-10	1	
9-21	R2			Allen Bradley Type G	POTENTIOMETER, 50K, 1/2W MEC SPN P-02-10	1	
9-22	R3, R4			Allen Bradley JA1L040S102UC	POTENTIOMETER, 1K, 2W, Linear Taper MEC SPN P-02-27	2	
9-23	R5-R12			MIL RC20GF241J	RESISTOR, Fixed Composition, 240 Ohms, ±5%, 1/2W	8	
9-24	R13-R16			MIL RC20GF621J	RESISTOR, Fixed Composition, 620 Ohms, ±5%, 1/2W	4	
9-25	R17			I.R.C. Type BW-2	RESISTOR, 4.7 Ohms, ±5%, 2W	1	
9-26	R18			I.R.C. Type BW-2	RESISTOR, 10 Ohm, ±5%, 2W	1	
9-27	R19			I.R.C. Type BW-2	RESISTOR, 56 Ohm, ±5%, 2W	1	
9-28	S1-S4			Centralab PA2015	SWITCH, Rotary, Non-Shorting, Ceramic MEC SPN S-01-15	4	
9-29	S5			Cutler Hammer 8906K832	SWITCH, Toggle, DPDT MEC SPN S-01-59	1	
9-30	S6			Fenwal 17000	THERMOSTAT MEC SPN S-01-119	1	
9-31	T1, T2			Triad HS-56	TRANSFORMER MEC SPN T-04-14	2	
9-32	T3			MEC 1-110	TRANSFORMER	1	
9-33	TJ1-TJ8			H.H. Smith 1501-113	TEST JACK MEC SPN T-02-01	8	
9-34	XF1			Bussman HKP	FUSE HOLDER MEC SPN F-01-04	1	
9-35	XI1-XI4			Dialco 7538-XP50	SOCKET, Cartridge Connector MEC SPN L-02-12	4	
9-36	XI5			Dialco 514001-111	INDICATOR HOLDER MEC SPN L-02-13	1	

1	2	3		4	5	6	7
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
9-37	XN1-XN5			MEC 14-101	SOCKET, 16 Pin	5	
9-38				Eldema 11D-50284	CARTRIDGE FASTENER, Speedclip (29 Finish) MEC SPN L-02-38	4	
9-39				Whitso K-105	KNOB MEC SPN K-01-01	4	

CHAPTER VIII

WIRE LIST

INDEX

WIRE NO.	REFERENCE TERMINAL	PAGE DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	J1	7-9		Keyer #1		
	J2	10-12		Keyer #2		
	J3	13-15		Keyer #3		
	J4	16-18		Keyer #4		
	J5	19-20		Test-Control		
	J6	21-22		Detector A		
	J7	23-24		Detector B		
	J8	25-26		Variable Delay SR. A		
	J9	27-28		Variable Delay SR. B		
	J10	29-30		Power Control		
	J11	53 & 54		Recorder Control		
	J12	Not Used				
	J13	31-33		Power Supply A		
	J14	34-36		Power Supply B		
	J15	4		Power Connector		
	J16	6		Output Connector		
	J17	5		Input Connector		
	J18	55		B-GE/IP Inputs		
	J19	56		Recorder Lines		
	J20	57		DLA Connector		

NOTES:

INDEX

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	+12V (A)	37				
	0V (A)	38				
	-20V (A)	39				
	-85V (A)	40				
	+12V (B)	41				
	0V (B)	42				
	-20V (B)	43				
	-85V (B)	44				

NOTES:

INDEX

WIRE NO.	REFERENCE	PAGE	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	SW1	45		Power Switch		
	XF1	46		Fuse		
	XF2	47		Fuse		
	XI1	48		Power on Indicator		
	TB1	49		Terminal Board		
	BL1	50		Blower		
	AC Switched	51				
	AC Common	52				

NOTES:

AC CONNECTOR J15

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	SW1-2	Jumper	AC Hot (Input)	14	S
	B	SW1-5	Jumper	AC Common	14	W
	C					
	D					
	E	Frame		Frame Ground	14	BK

NOTES: MS3102A-18-11P

INPUT CONNECTOR
J17

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J5-1	2	Shift Request	22	BR
	B					
	C	J5-3	2	Select & Ready	22	Y
	D					
	E	J5-4	2	Data	22	G
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					
	N	OV- (13)B	1	System Ground	14	BK
	O					
	P					

NOTES: MS3102A-24-7P

OUTPUT CONNECTOR
J16

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J1-5	2	Data Out Transmitter 1	RG174U	
	B	J1-6	2	Shield of J16-A & J16-C		
	C	J1-7	2	Data Out Transmitter 1	RG174U	
	D					
	E	J2-5	2	Data Out Transmitter 2	RG174U	
	F	J2-6	2	Shield of J16-E &J16-G		
	G	J2-7	2	Data Out Transmitter 2	RG174U	
	H					
	J	J3-5	2	Data Out Transmitter 3	RG174U	
	K	J3-6	2	Shield of J16-J & J16-L		
	L	J3-7	2	Data Out Transmitter 3	RG174U	
	M	J4-6	2	Shield of J16-N & J16-U		
	N	J4-7	2	Data Out Transmitter 4	RG174U	
	P					
	R					
	S					
	T					
	U	J4-5	2	Data Out Transmitter 4	RG174U	
	V					

NOTES: MS3102A-22-14S

J1

KEYER 1

	WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
		1	J8-11	2	Data	22	BL
6 3		2	J8-14	2	SOW	22	G
		3	J8-8	2	EOW	22	W/BL
		4					
		5	J16-A	2	Data Out Transmitter 1	RG174/U	
		6	J16-B	2	Shields of J1-5 & J1-7		
		7	J16-C	2	Data Out Transmitter 1	RG174/U	
4		8	J19-T	2	Keyer #1 Output	RG174/U	
4		9	J19-K	2	Keyer #1 Input	RG174/U	
		10					
4		11	J1-45	Jumper	0V (A)	22	BK
4		12	J2-12	2	Keyer Relay	20	W-G
		13					
		14					
		15					
		16					
		17					
		18					
		19					
		20					
		21					
		22					
		23					
		24					
		25					

NOTES:

J1

KEYER 1

	WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
		26					
		27					
		28					
		29					
		30					
		31					
		32					
		33					
		34					
		35					
		36					
		37					
		38					
		39	AC Com-1	1	AC Common	20	W
		40	AC Switched-1	1	AC Switched	20	W/S
		41	J10-18	1	+250V (1)	22	W/R
		42					
		43	+12V-1(A)	1	+12V (A)	20	R
		44	0V-1 (A)	1	0V (A)	20	BK
		45	0V-1 (A)	1	0V (A)	20	BK
4		45	J1-11	Jumper	0V (A)	22	BK
		46					
		47					
		48					
		49	-85V-1(A)	1	-85V (A)	20	W/BK

NOTES:

J1
KEYER 1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	50	Frame		Chassis Gnd	20	BK

NOTES:

J2
KEYER #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J8-10	2	Data	22	O
	2	J8-15	2	SOW	22	Y
	3	J8-9	2	EOW	22	G
	4					
	5	J16-E	2	Data Out Transmitter 2	RG174/U	
	6	J16-F	2	Shields of J2-5 & J2-7		
	7	J16-G	2	Data Out Transmitter 2	RG174/U	
	8	J19-V	2	Keyer #2 Output	RG174/U	
	9	J19-L	2	Keyer #2 Input	RG174/U	
	10					
	11	J2-45	Jumper	OV (A)	22	BK
	12	J3-12	2	Keyer Relay	20	W-G
	12	J1-12	2	Keyer Relay	20	W-G
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

Rev. 6/22/62

J2
KEYER #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39	AC Com-2	1	AC Common	20	W
	40	AC Switched-2	1	AC Switched	20	W/S
	41	J10-19	1	+250V (2)	22	W/R
	42					
	43	+12-2 (A)	1	+12V (A)	20	R
	44	0V-2 (A)	1	0V (A)	20	BK
	45	0V-2 (A)	1	0V (A)	20	BK
	45	J2-P1	Jumper	0V (A)	22	BK
	46					
	47					
	48					
	49	-85V-2(A)	1	-85V (A)	20	W/BK

NOTES:

J2
KEYER #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	50	Frame		Chassis Gnd	20	BK

NOTES:

J3
KEYER #3

	WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
		1	J9-11	2	Data	22	W/O
6 3		2	J9-14	2	SOW	22	G
		3	J9-8	2	EOW	22	G
		4					
		5	J16-J	2	Data Out Transmitter 3	RG174/U	
		6	J16-K	2	Shields of J3-5 & J3-7		
		7	J16-L	2	Data Out Transmitter 4		
4		8	J19-Z	2	Keyer #3 Output	RG174/U	
4		9	J19-W	2	Keyer #3 Input	RG174/U	
		10					
4		11	J3-45	Jumper	OV (B)	22	BK
4		12	J4-12	2	Keyer Relay	20	W-G
4		12	J2-12	2	Keyer Relay	20	W-G
		13					
		14					
		15					
		16					
		17					
		18					
		19					
		20					
		21					
		22					
		23					
		24					
		25					

NOTES:

J3
KEYER #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39	AC Com-3	1	AC Common	20	W
	40	AC Switched-3	1	AC Switched	20	W/S
	41	J10-20	1	+250V (3)	22	W/R
	42					
	43	+12V-1 (B)	1	+12V (B)	20	R
	44	OV-1 (B)	1	OV (B)	20	BK
	45	OV-1 (B)	1	OV (B)	20	BK
	45	J3-11	Jumper	OV (B)	22	BK
	46					
	47					
	48					
	49	-85V-1 (B)	1	-85V (B)	20	BK

NOTES:

J3 KEYER #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	50	Frame		Chassis Gnd	20	BK

NOTES:

J4 KEYER #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J9-10	2	Data	22	W/G
	2	J9-15	2	SOW	22	G
	3	J9-9	2	EOW	22	O
	4					
	5	J16-U	2	Data Out Transmitter 4	RG174/U	
	6	J16-M	2	Shields of J4-5 & J4-7		
	7	J16-N	2	Data Out Transmitter 4	RG174/U	
	8					
	9					
	10					
	11	J4-45	Jumper	OV (B)	22	BK
	12	J11-49	2	Keyer Relay	20	W-G
	12	J3-12	2	Keyer Relay	20	W-G
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J4
KEYER #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39	AC Com-4	1	AC Common	20	W
	40	AC Switched-4	1	AC Switched	20	W/S
	41	J10-21	1	+250V (4)		W/R
	42					
	43	+12-2 (B)	1	+12V (B)	20	R
	44	0V-2 (B)	1	0V (B)	20	BK
	45	0V-2 (B)	1	0V (B)	20	BK
	45	J4-11	Jumper	0V (B)	22	BK
	46					
	47					
	48					
	49	-85V-2(B)	1	-85V (B)	20	W/BK

NOTES:

J4
KEYER #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	50	Frame		Chassis Gnd	20	BK

NOTES:

J5
TEST - CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-A	2	Shift Request	22	BR
	2	J6-10	2	Relay Drive	22	O
	3	J17-C	2	Select & Ready	22	Y
	4	J17-E	2	Data	22	G
	5	J6-9	2	Reset	22	BL
	6	J6-1	2	Select & Ready (A)	22	O
	7	J7-1	2	Select & Ready (B)	22	W/O
	8	J6-2	2	Data (A)	22	W/Y
	9	J7-2	2	Data (B)	22	W/G
	10	J6-3	2	Shift Trigger	22	W/BL
	11	J7-4	2	Shift	22	W/V
	12	J6-8	2	Shift	22	BL
	13	J7-3	2	Shift Trigger	22	O
	14	J7-18	2	Test Zero Data Level	22	BL
	15					
	16	AC Common-5	1	AC Common	20	W
	17	AC Switched-5	1	AC Switched	20	W/S
	18	J7-43	1	-10V (B)	22	V
	19					
	20					
	21	J6-4	2	Sample Trigger A	22	Y
	22	J7-8	2	Sample Trigger B	22	G
	23	J8-1	2	C.D. Trigger	22	BL
	24	J9-1	2	C. D. Trigger	22	O
	25					

NOTES:

J5
TEST - CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30	J7-38	2	Shift Request	22	W/O
	31	J7-34	2	Test Select & Ready	22	W/Y
	32	J7-35	2	Test Select & Ready Reset	22	W/BL
	33	J7-36	2	Start Pulse	22	Y
	34	-85V-3 (B)	1	-85V (B)	20	W/BK
	35	-20V-3 (B)	1	-20V (B)	20	S
	36	-20V-3 (B)	1	-20V (B)	20	S
	37	0V-3 (B)	1	0V (B)	20	BK
	38	0V-3 (B)	1	0V (B)	20	BK
	39	+12V-3 (B)	1	+12V (B)	20	R
	40					
	41	J6-43	1	-10V (A)	20	V
	42					
	43					
	44	+12V-3 (A)	1	+12V (A)	20	R
	45	0V-3A	1	0V (A)	20	BK
	46	0V-3A		0V (A)	20	BK
	47	-20-3 (A)	1	-20V (A)	20	S
	48	-20-3 (A)	1	-20V (A)	20	S
	49	-85-3 (A)	1	-85V (A)	20	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J6
DETECTOR A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-6	2	Select & Ready (A)	22	O
	2	J5-8	2	Data (A)	22	W/Y
	3	J5-10	2	Shift Trigger	22	W/R
	4	J5-21	2	Sample Trigger (A)	22	Y
	5	J8-2	2	Sample	22	O
	6	J8-4	2	Art One	22	G
	7	J8-7	2	EOW	22	BR
	8	J5-12	2	Shift	22	BL
	9	J5-5	2	Reset	22	BL
	10	J5-2	2	Relay Drive	22	O
	11	J8-3	2	Sample	22	W/G
	12					
	13					
	14					
	15					
	16					
6	17	J8-13	2	SOW To S.R.	22	Y
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J6
DETECTOR A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J7-38	2	Shift Request	22	W/O
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43	J5-41	1	-10V (A)	20	V
	44	12V-4 (A)	1	+12V (A)	20	R
	45	0V-4(A)	1	0V (A)	20	BK
	46	0V-4(A)	1	0V (A)	20	BK
	47	-20V-4(A)	1	-20V (A)	20	S
	48	-20V-4(A)	1	-20V (A)	20	S
	49					
	50	Frame		Chassis Gnd	20	BK

NOTES:

J7
DETECTOR B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-7	2	Select & Ready (B)	22	W/O
	2	J5-9	2	Data (B)	22	W/G
	3	J5-13	2	Shift Trigger	22	O
	4	J5-11	2	Shift	22	W/V
	5	J9-3	2	Sample	22	BR
	6	J9-7	2	EOW	22	BL
	7	J9-4	2	Art One	22	Y
	8	J5-22	2	Sample Trigger (B)	22	G
	9	J9-2	2	Sample	22	W/BR
	10					
	11					
	12					
	13					
6 3	14					
6 3	15					
6 3	16					
6 3	17	J9-13	2	SOW to S.R.	22	Y
6	18	J5-14	2	Test Zero Data Level	22	BL
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J7
DETECTOR B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J5-31	2	Test Select & Ready	22	W/O
	35	J5-32	2	Test Select & Ready Reset	22	W/G
	36	J5-33	2	Start Pulse	22	W/BL
	37					
	38	J5-30	2	Shift Request	22	W/O
	38	J6-34	2	" "	22	W/O
	39					
	40					
	41					
	42					
	43	J5-18	1	-10V (B)	22	V
	44	+12V-4(B)	1	+12V (B)	20	R
	45	0V-4 (B)	1	0V (B)	20	BK
	46	0V-4 (B)	1	0V (B)	20	BK
	47	-20V-4 (B)	1	-20V (B)	20	S
	48	-20V-4 (B)	1	-20V (B)	20	S
	49					
	50	Frame		Chassis Gnd	20	BK

NOTES:

J8

DUAL S.R. A.

	WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
		1	J5-23	2	C. D. Trigger	22	BL
		2	J6-5	2	Sample	22	O
		3	J6-11	2	Sample	22	W/G
		4	J6-6	2	Art Ones	22	G
		5					
6		6			Core Drive		
		7	J6-7	2	EOW	22	BR
6		8	J1-3	2	EOW To Keyer	22	W/BL
6		9	J2-3	2	EOW To Keyer	22	G
6		10	J2-1	2	DataTo Keyer	22	O
6		11	J1-1	2	Data To Keyer	22	BL
		12					
6		13	J6-17	2	SOW to S.R.	22	Y
6		14	J1-2	2	SOW to Keyer	22	G
6		15	J2-2	2	SOW to Keyer	22	Y
		16					
		17					
		18					
		19					
		20					
		21					
		22					
		23					
		24					
		25					

NOTES:

J8

DUAL S.R. A.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12-5 (A)	1	+12V (A)	20	R
	45	OV-5 (A)	1	OV (A)	20	BK
	46	OV-5 (A)	1	OV (A)	20	BK
	47	-20-5 (A)	1	-20V (A)	20	S
	48	-20-5 (A)	1	-20V (A)	20	S
	49	-85V-5(A)	1	-85V (A)	20	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J9
DUAL S. R. B.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-24	2	C. D. Trigger	22	O
	2	J7-9	2	Sample	22	W/BR
	3	J7-5	2	Sample	22	BR
	4	J7-7	2	Art One	22	Y
	5					
	6					
	7	J7-6	2	EOW	22	BL
6	8	J3-3	2	EOW To Keyer	22	G
6	9	J4-3	2	EOW To Keyer	22	O
6	10	J4-1	2	Data To Keyer	22	W/G
6	11	J3-1	2	Data To Keyer	22	W/O
	12					
6	13	J7-17	2	SOW to S.R.	22	Y
6	14	J3-2	2	SOW to Keyer	22	G
6	15	J4-2	2	SOW to Keyer	22	G
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J9
DUAL S.R.B.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V-5(B)	1	+12V (B)	20	R
	45	0V-5(B)	1	0V (B)	20	BK
	46	0V-5(B)	1	0V (B)	20	BK
	47	-20V-5(B)	1	-20V (B)	20	S
	48	-20V-5(B)	1	-20V (B)	20	S
	49	-85V-5(B)	1	-85V (B)	20	W/BK
	50	Frame		Chassis Gnd	22	BK

NOTES:

J10
POWER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5	AC Common-6	1	AC Common	20	W
	6					
	7		1	AC Fused		
	8	XF1-2	1	AC Fused	18	S
	9		1	AC Fused		
	10	XF1-2	1	AC Fused	18	S
	11					
	12	AC Switched-9	1	AC Switched	18	W/S
	13					
	14	AC Switched-10	1	AC Switched	18	W/S
	15					
	16					
	17					
	18	J1-41	1	+250V (1)	22	W/R
	19	J2-41	1	+250V (2)	22	W/R
	20	J3-41	1	+250V (3)	22	W/R
	21	J4-41	1	+250V (4)	22	W/R
	22					
	23					
	24					
	25					

NOTES:

J10
POWER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	+12V-6(A)	1	+12V (A)	22	R
	35	-20V-6(A)	1	-20V (A)	22	S
	36	-85V-6(A)	1	-85V (A)	22	W/BK
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V-6(B)	1	+12V (B)	22	R
	45	0V-6(A)	1	0V (A)	22	BL
	46					
	47	-20V-6(B)	1	-20V (B)	22	S
	48					
	49	-85V-6(B)	1	-85V (B)	22	W/BK
	50	Frame		Chassis Gnd	22	BK

NOTES:

Rev. 6/15/61

J-13
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC Common Bus -7	1	AC Common	20	W
	2	AC Common Bus - 7	1	AC Common	20	W
	3					
	4	AC Switched Bus 6	1	AC Switched	20	W/S
	5	AC Switched Bus -6	1	AC Switched	20	W/S
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					

NOTES:

J-13
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34			+12V, Unregulated		
	35			-20V, Unregulated		
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V-10(A)	1	+12V (A)	20	R
	45	0V-10(A)	1	0V (A)	20	BK
	46	0V-10(A)	1	0V (A)	20	BK
	47	-20V-10(A)	1	-20V (A)	20	S
	48	-20V-10(A)	1	-20V (A)	20	S

NOTES:

J-13
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	49	-85V-10(A)	1	-85V (A)	20	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J-14
POWER SUPPLY "B"

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC Common Bus 9	1	AC Common	20	W
	2	AC Common Bus 9		AC Common	20	W
	3					
	4	AC Switched Bus 7		AC Switched	20	W/S
	5	AC Switched Bus 7		AC Switched	20	W/S
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					

NOTES:

J14
POWER SUPPLY "B"

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34			+12V, Unregulated Output		
	35			-20V, Unregulated Output		
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12-10(B)	1	+12V (B)	20	R
	45	0V-10(B)	1	0V (B)	20	BK
	46	0V-10(B)	1	0V (B)	20	BK
	47	-20V-10(B)	1	-20V (B)	20	S
	48	-20V-10(B)	1	-20V (B)	20	S

NOTES:

J-14
POWER SUPPLY "B"

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	49	-85V-10(B)	1	-85V (B)	20	W/BK
	50	Frame		Chassis Ground	20	BK

NOTES:

+12V BUS "A"

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-43	1	+12V (A)	20	R
	2	J2-43			20	
	3	J5-44			20	
	4	J6-44			20	
	5	J8-44			20	
	6	J10-34			22	
	7					
	8					
	9					
	10	J13-44			20	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

OV BUS "A"

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-44	1	OV (A)	20	BK
	1	J1-45			20	
	2	J2-44			20	
	2	J2-45			20	
	3	J5-45			20	
	3	J5-46			20	
	4	J6-45			20	
	4	J6-46			20	
	5	J8-45			20	
	5	J8-46			20	
	6	J10-45			22	
	7					
	7					
	8					
	9					
	10	J13-45			20	
	10	J13-46			20	
	11					
	12	OV-12(B)		OV	14	BK
	13	Frame		Chassis Gnd	14	BK
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

-20V BUS 'A'

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1		1	-20V (A)		S
	2					
	3	J5-47			20	
	3	J5-48			20	
	4	J6-47			20	
	4	J6-48			20	
	5	J8-47			20	
	5	J8-48			20	
	6	J10-35			22	
	7					
	7					
	8					
	9					
	10	J13-47			20	
	10	J13-48			20	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

-85V BUS 'A'

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-49	1	-85V (A)	20	W/BK
	2	J2-49			20	
	3	J5-49			20	
	4					
	5	J8-49			20	
	6	J10-36			22	
	7					
	8					
	9					
	10	J13-49			20	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

+ 12V Bus B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-43	1	+12V (B)	20	R
	2	J4-43			20	
	3	J5-39			20	
	4	J7-44			20	
	5	J9-44			20	
	6	J10-44			22	
	7				20	
	8					
	9					
	10	J14-44			20	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

OV BUS B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-44	1	OV (B)	20	BK
	1	J3-45				
	2	J4-44				
	2	J4-45				
	3	J5-37				
	3	J5-38				
	4	J7-45				
	4	J7-46				
	5	J9-45				
	5	J9-46				
	6	J11-45				
	7					
	7					
	8					
	9					
	10	J14-45				
	10	J14-46				
	11					
	12	OV-12(A)		OV	14	BK
	13	J17-N	1	System Ground	14	BK
	14	J19-C	2	OV (B)	20	BK
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

-85V BUS B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-49	1	-85V (B)	20	W/BK
	2	J4-49			20	
	3	J5-34			20	
	4					
	5	J9-49			20	
	6	J10-49			22	
	7					
	8					
	9					
	10	J14-49			20	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

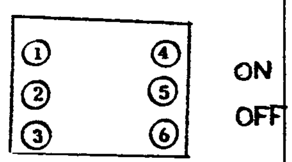
-20V BUS B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1		1	-20V (B)		S
	2					
	3	J5-35			20	
	3	J5-36			20	
	4	J7-47			20	
	4	J7-48			20	
	5	J9-47			20	
	5	J9-48			20	
	6	J10-47			22	
	7					
	7					
	8					
	9					
	10	J14-47			20	
	10	J14-48			20	
	11					
	12					
	13					
	14	J19-B	2	-20V (B)	20	S
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

SW1

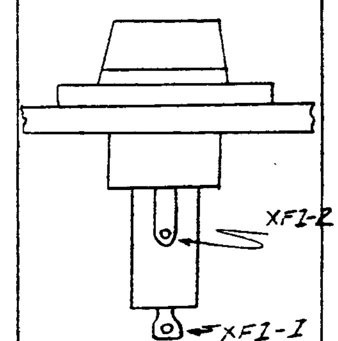
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	XF1-1	Jumper	AC Input	14	S
	2	J15-A	Jumper	AC Hot	14	S
	3					
	4	XF2-1	Jumper	AC Common	14	W
	5	J15-B	Jumper	AC Common	14	W
	6					



NOTES:

XF1
FUSE 1

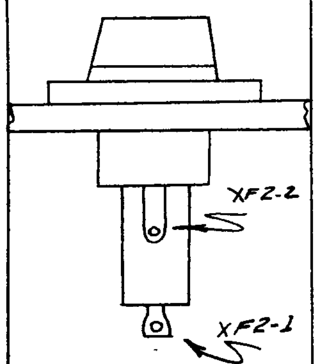
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-1	Jumper	AC Input	14	S
	2	XI1-1	Jumper	AC Fused	20	S
	2	J10-8	1	AC Fused	18	S
	2	J10-10	1	AC Fused	18	S



NOTES:

XF2
FUSE 2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-4	Jumper	AC Common	14	W
	2	XI1-2	Jumper	AC Common	20	W
	2	AC Com-10	1	AC Common	14	W



NOTES:

POWER INDICATOR
XI1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	XF1-2	Jumper	AC Fused	20	S
	2	XF2-2	Jumper	AC Common (Fused)	20	W

NOTES:

TB1
BLOWER
TERMINAL STRIP

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	BL1-1	Direct	AC Switched	18	W-S
	1	AC SW BUS	1	AC Switched	18	W-S
	2	BL1-2	Direct	AC Common	18	W
	2	AC COM BUS	1	AC Common	18	W

NOTES:

BL1
BLOWER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	TB1-1	Direct	AC Switched	18	W-S
	2	TB1-2	Direct	AC Common	18	W

NOTES:

AC SWITCHED BUS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-40	1	AC Switched	20	W/S
	2	J2-40			20	W/S
	3	J3-40			20	
	4	J4-40			20	
	5	J5-17			20	
	6	J13-4			20	
	6	J13-5			20	
	7	J14-4			20	
	7	J14-5			20	
	8	TB1-1			18	
	9	J10-12		AC Switched	18	W/S
	10	J10-14		AC Switched	18	W/S
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

AC COMMON BUS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-39	1	AC Common	20	W
	2	J2-39			20	
	3	J3-39			20	
	4	J4-39			20	
	5	J5-16			20	
	6	J10-5			20	
	7	J13-1			20	
	7	J13-2			20	
	8	TB1-2			18	
	9	J14-1			20	
	9	J14-2			20	
	10	XF2-2			14	
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

J11 RECORDER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J18-A	2	B-GE Input Line #1	RG174/U	
	2					
	3	J18-B	2	B-GE Input Line #1	RG174/U	
	4					
	5	J20-A	2	DLA #1 Input	RG174/U	
	6					
	7	J20-B	2	DLA #1 Input	RG174/U	
	8					
	9	J19-E	2	Tape Output #1	RG174/U	
	10	Rack Gnd		Shield of J11-9		
	11					
	12	J18-C	2	B-GE Input Line #2	RG174/U	
	13					
	14	J18-D	2	B-GE Input Line #2	RG174/U	
	15					
	16	J20-C	2	DLA #2 Input	RG174/U	
	17					
	18	J20-D	2	DLA #2 Input	RG174/U	
	19					
	20	J19-F	2	Tape Output #2	RG174/U	
	21	Rack Gnd		Shield of J11-20		
	22					
	23	J18-E	2	IP Input Line #1	RG174/U	
	24					
	25	J18-F	2	IP Input Line #1	RG174/U	

NOTES: Gnd. All Coax to Rack

J11 RECORDER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27	J20-E	2	DLA #3 Input	RG174/U	
	28					
	29	J20-F	2	DLA #3 Input	RG174/U	
	30					
	31	J19-G	2	Tape Output #3	RG174/U	
	32	Rack Gnd		Shield of J11-31		
	33					
	34	J18-G	2	IP Input Line #2	RG174/U	
	35					
	36	J18-H	2	IP Input Line "2	RG174/U	
	37					
	38	J20-G	2	DLA #4 Input	RG174/U	
	39					
	40	J20-H	2	DLA #4 Input	RG174/U	
	41					
	42	J19-H	2	Tape Output #4	RG174/U	
	43	Rack Gnd		Shield of J11-42		
	44					
	45	0V-6(B)	2	0V	20	BK
	46	J19-A	2	Recorder Playback Confirm	20	Y
	47					
	48					
	49	J4-12	2	Keyer Relay	20	W-G
	50					

NOTES: Gnd. All Coax to Rack

J18
B-GE/IP INPUTS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J11-1	2	B-GE Input Line #1	RG174/U	
	B	J11-3	2	B-GE Input Line #1	RG174/U	
	C	J11-12	2	B-GE Input Line #2	RG174/U	
	D	J11-14	2	B-GE Input Line #2	RG174/U	
	E	J11-23	2	IP INput Line #1	RG174/U	
	F	J11-25	2	IP Input Line #1	RG174/U	
	G	J11-34	2	IP Input Line #2	RG174/U	
	H	J11-36	2	IP Input Line #2	RG174/U	
	J					
	K					
	L					

NOTES: MS3102A-24-20P

J19
RECORDER LINES

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J11-46	2	Recorder Playback Confirm	20	Y
	B	-20V-14(B)	2	-20V (B)	20	S
	C	0V-14(B)	2	0V (B)	20	BK
	D					
	E	J11-9	2	Tape Output #1	RG174/U	
	F	J11-20	2	Tape Output #2	RG174/U	
	G	J11-31	2	Tape Output #3	RG174/U	
	H	J11-42	2	Tape Output #4	RG174/U	
	J					
	K	J1-9	2	Keyer #1 Input	RG174/U	
	L	J2-9	2	Keyer #2 Input	RG174/U	
	M					
	N					
	P					
	R	Frame		Rack Gnd	18	BK
	S					
	T	J1-8	2	Keyer #1 Output	RG174/U	
	U					
	V	J2-8	2	Keyer #2 Output	RG174/U	
	W	J3-9	2	Keyer #3 Input	RG174/U	
	X					
	Y					
	Z	J3-8	2	Keyer #3 Output	RG174/U	

NOTES: MS3102A-32-13P

J20
DLA CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J11-5	2	DLA #1 Input	RG174/U	
	B	J11-7	2	DLA #1 Input	RG174/U	
	C	J11-16	2	DLA #2 Input	RG174/U	
	D	J11-18	2	DLA #2 Input	RG174/U	
	E	J11-27	2	DLA #3 Input	RG174/U	
	F	J11-29	2	DLA #3 Input	RG174/U	
	G	J11-38	2	DLA #4 Input	RG174/U	
	H	J11-40	2	DLA #4 Input	RG174/U	
	J					
	K					

NOTES: MS3102A-24-21P

CHAPTER IX

SCHEMATICS AND DIAGRAMS

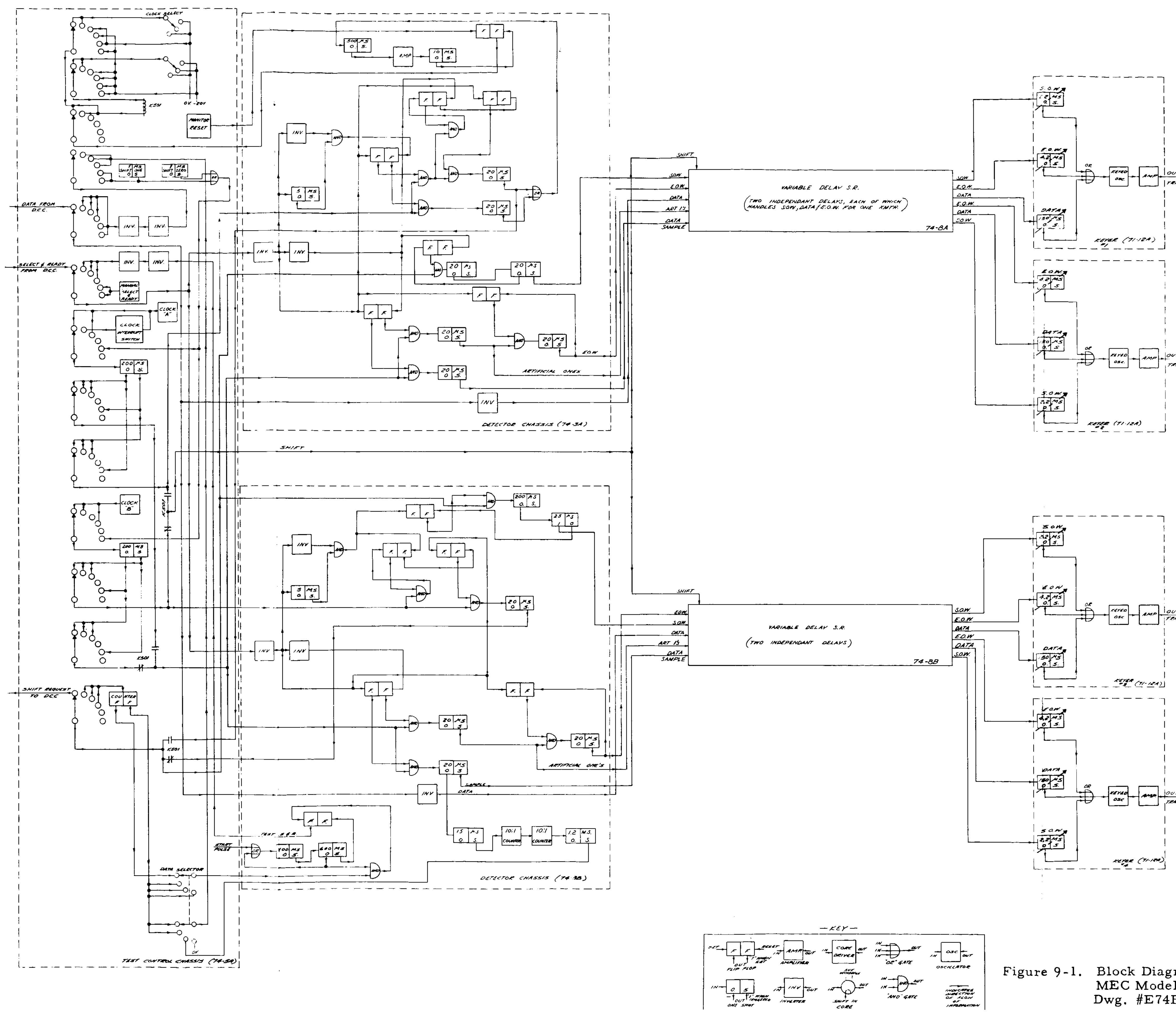


Figure 9-1. Block Diagram
MEC Model 74 Data Transmitter
Dwg. #E74B1A

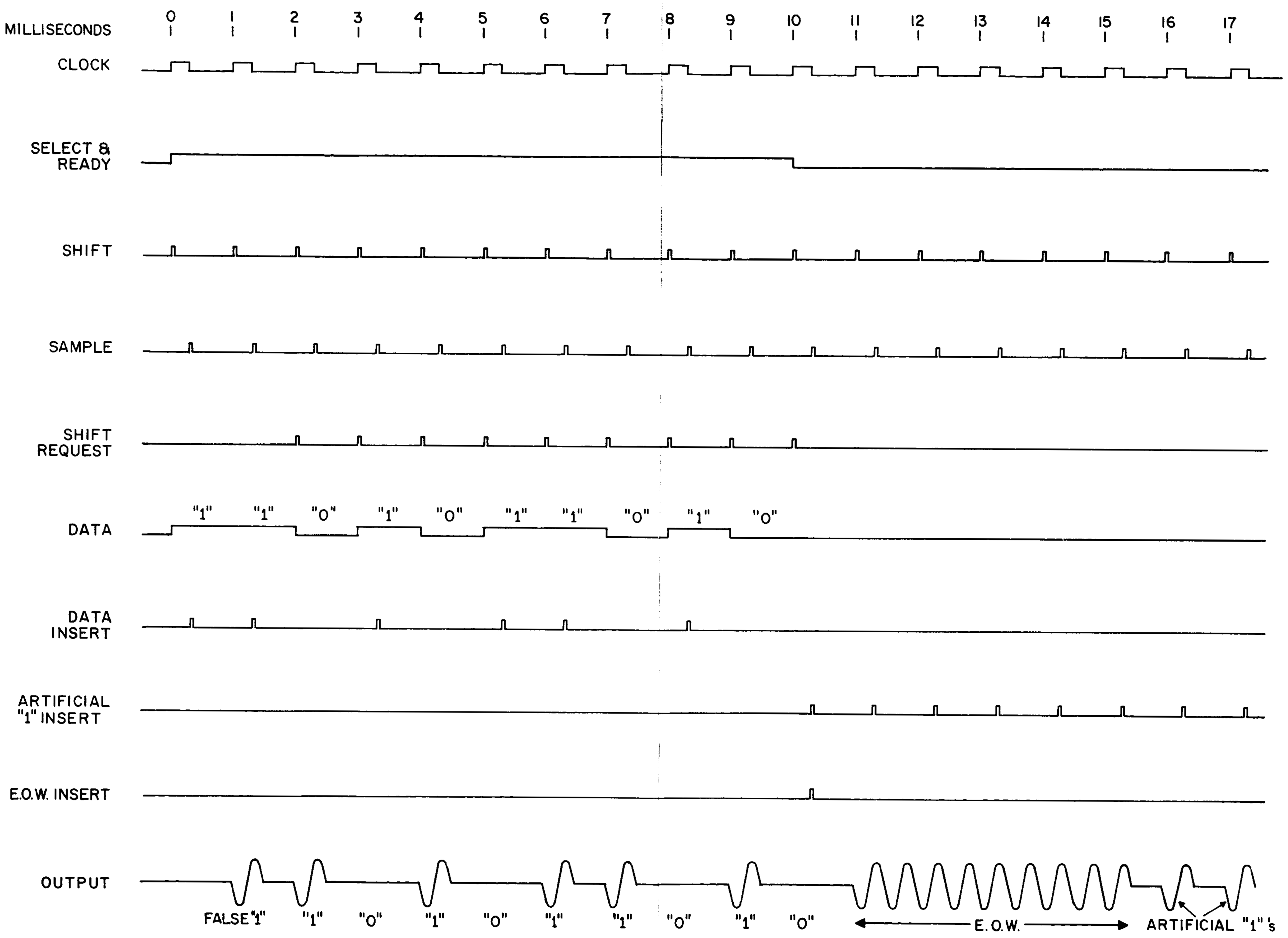


Figure 9-2. Timing Diagram

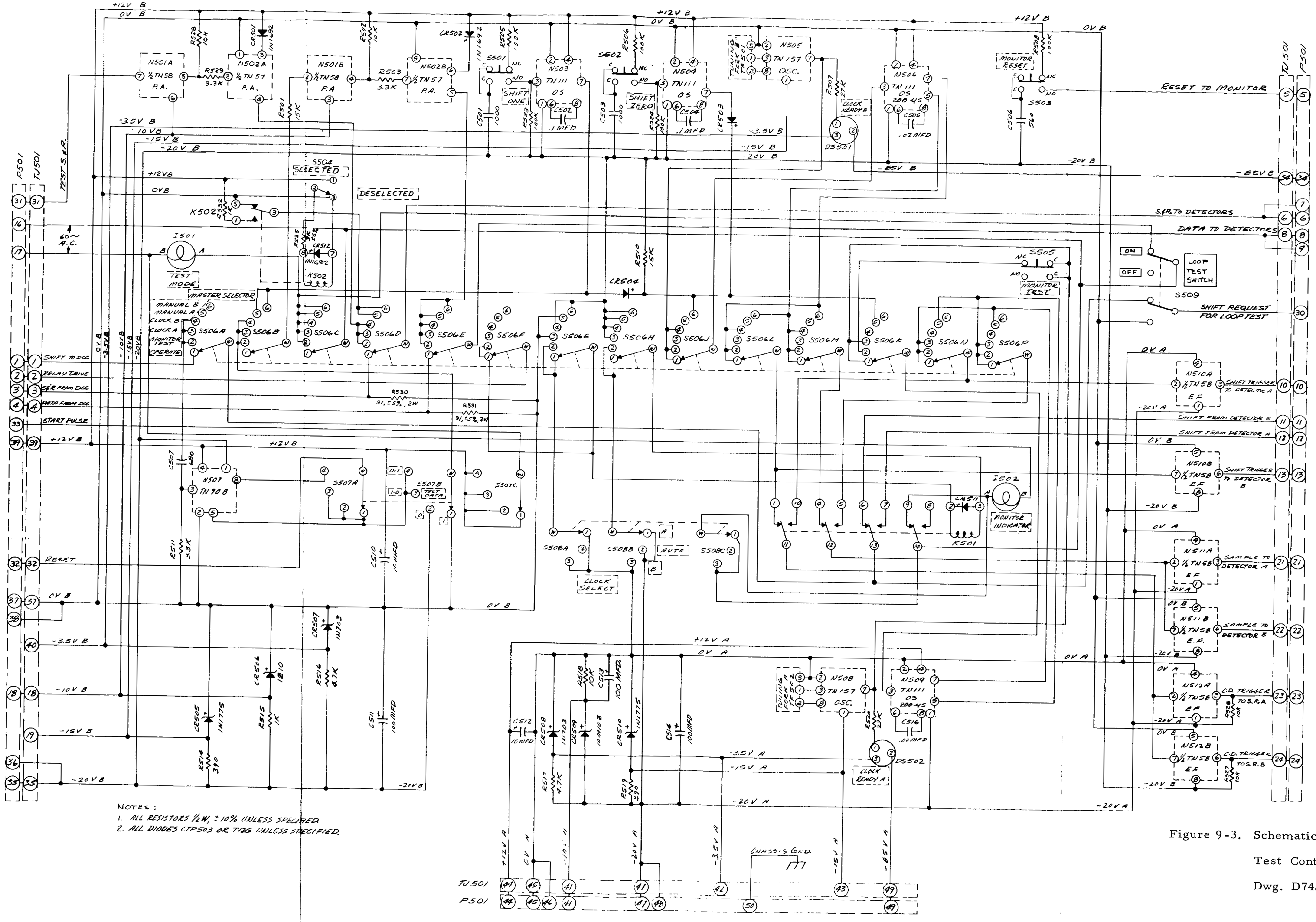
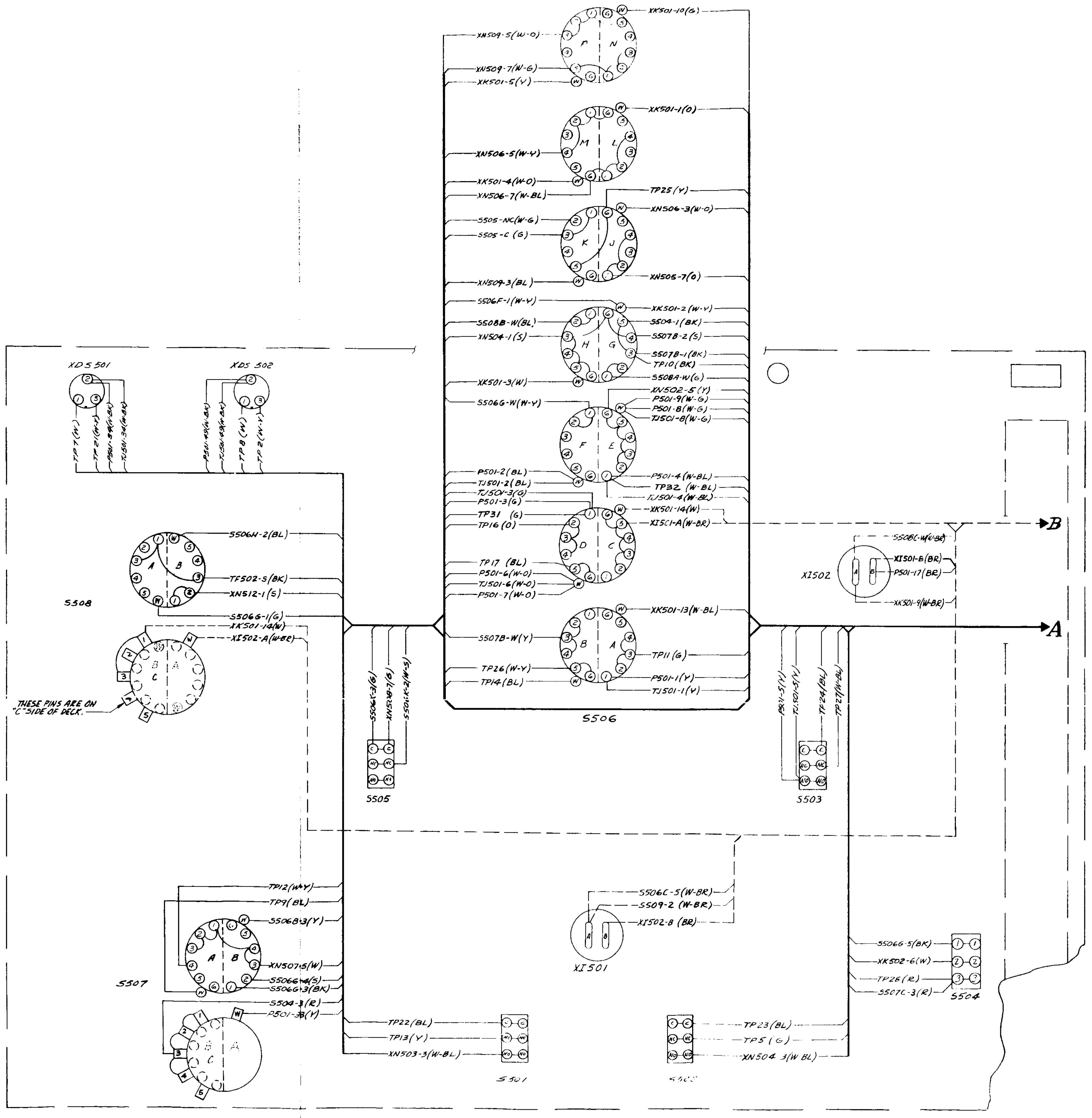
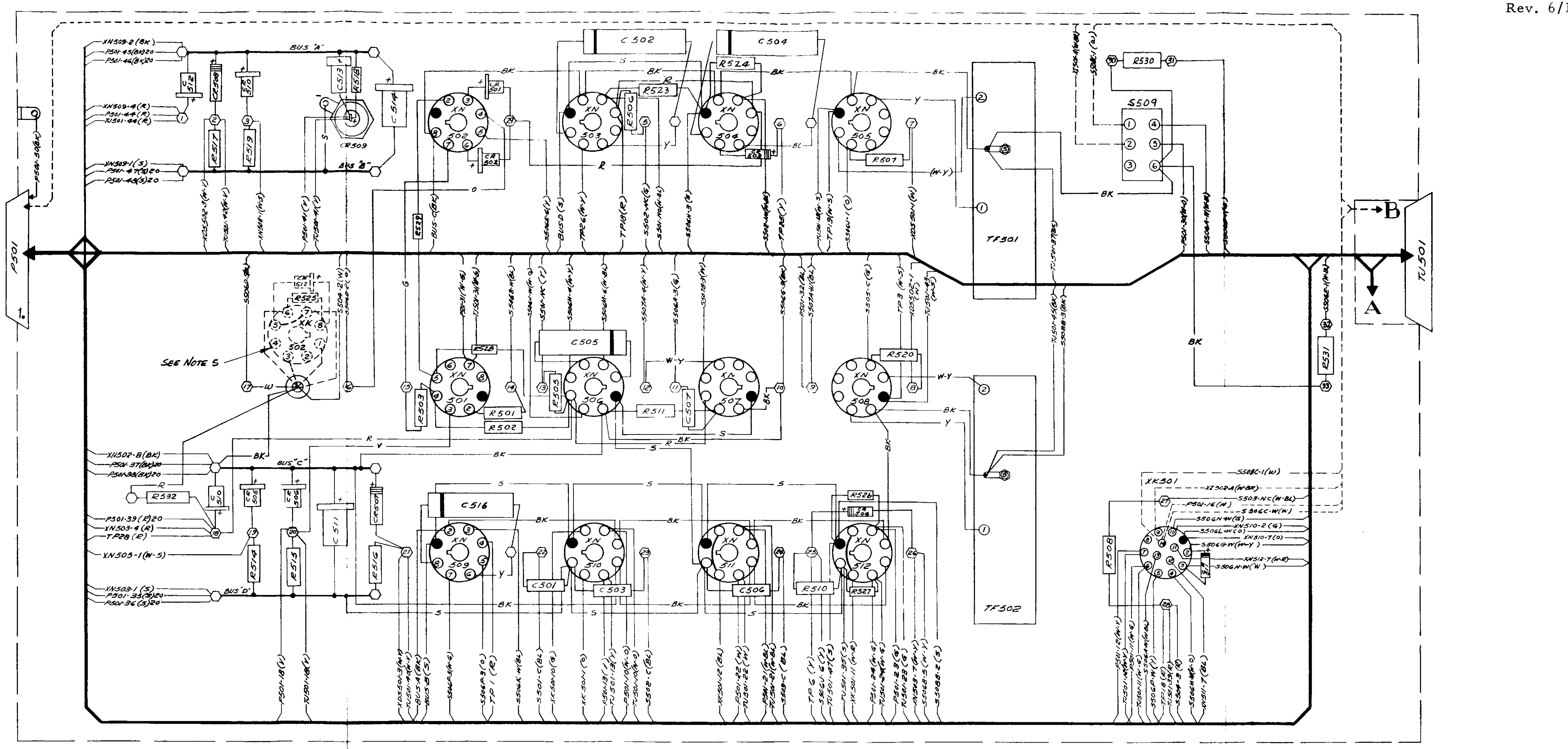


Figure 9-3. Schematic
Test Control Chassis
Dwg. D74S5A



NOTES:
1. ---- DENOTES AC LEADS.
2. TWIST AC LEADS IN PAIRS.
3. ALL WIRES TO BE 22 GA UNLESS SPECIFIED.

Figure 9-4. Wiring Diagram
Test Control Chassis
Dwg. D74W5A, Sheet 1

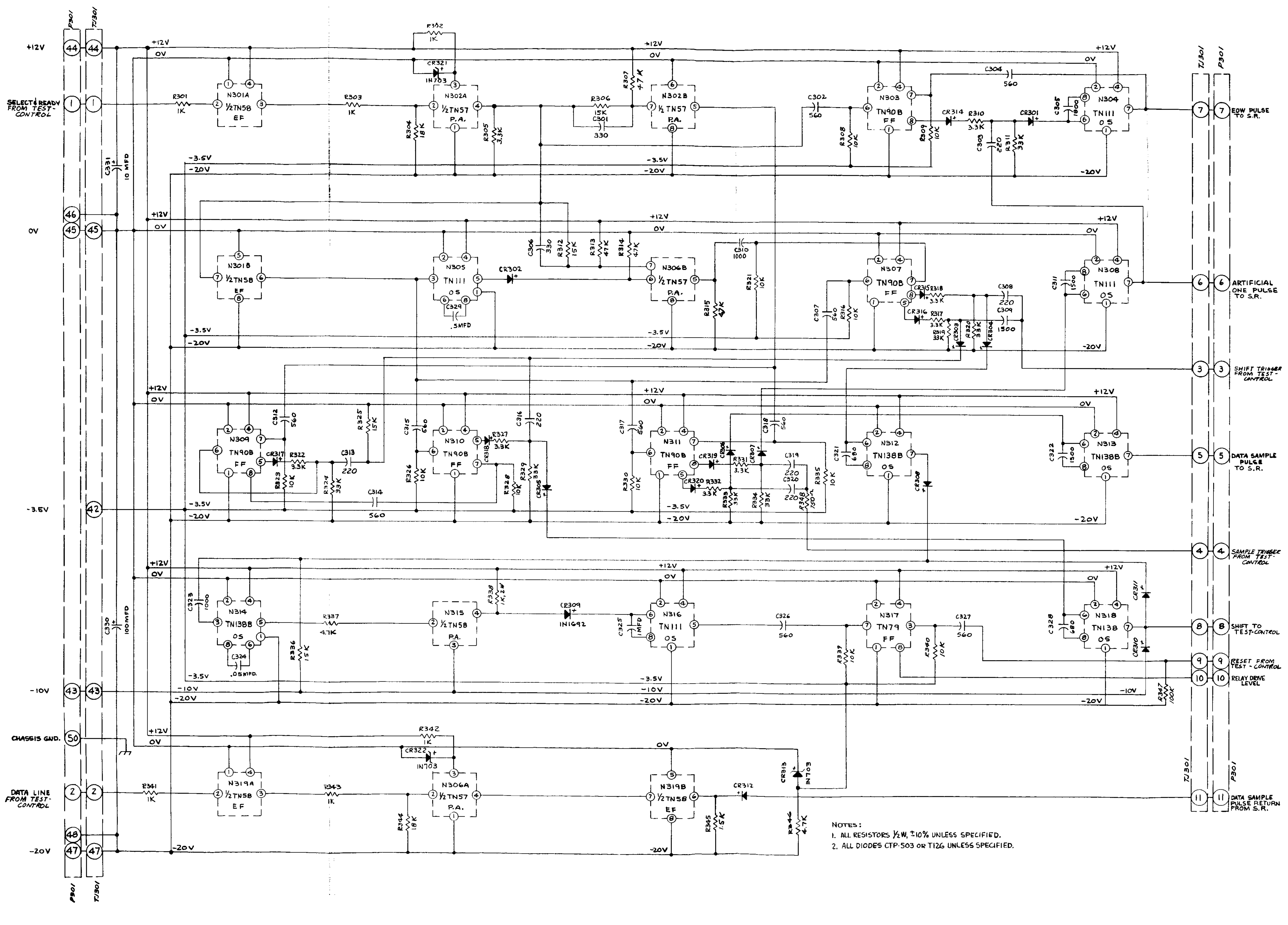


P501							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	S506A-1	SHIFT TO DCC	Y	26			
2	S506F-W	RELAY DRIVE	BL	27			
3	S506D-1	S&R FROM DCC	G	28			
4	S506E-1	DATA FROM DCC	(W-BL)	29			
5	S503-NO	RESET TO MONITOR	Y	30	S509-5	SHIFT REQUEST FOR LOOP TEST	(W-O)
6	S506D-W	S.R. TO DETECTORS	(W-O)	31	XN501-7	TEST SELECT & READY	(W-G)
7	S506D-W	S.R. TO DETECTORS	(W-O)	32			
8	S506E-W	DATA TO DETECTORS	(W-G)	33	S507C-W	START PULSE	Y
9	S506E-W	DATA TO DETECTORS	(W-G)	34	XDS 501-2	-85V "B"	(W-BK)
10	XN510-3	SHIFT TRIG. TO DET. "A"	(W-O)	35	BUS "D"	-20V "B"	(S) 20
11	XK501-6	SHIFT FROM DET. "B"	(W-G)	36	BUS "D"	-20V "B"	(S) 20
12	XK501-7	SHIFT FROM DET. "A"	(W-Y)	37	BUS "C"	0V "B"	(BK) 20
13	XN510-6	SHIFT TRIG. TO DET. "B"	Y	38	BUS "C"	0V "B"	(BK) 20
14				39	TP 18	+12V "B"	(R) 20
15				40			
16	XK501-14	60~ A.C.	W	41	CR509(+)	-10V "A"	(V)
17	XI502-B	60~ A.C.	BR	42			
18	TP 20	-10V "B"	V	43			
19				44	TP1	+12V "A"	R
20				45	BUS "A"	0V "A"	(BK) 20
21	XN511-3	SAMPLE TO DET. "A"	(W-BL)	46	BUS "A"	0V "A"	(BK) 20
22	XN511-6	SAMPLE TO DET. "B"	W	47	BUS "B"	-20V "A"	(S) 20
23	XN512-3	C.D. TRIG. TO S.R. "A"	G	48	BUS "B"	-20V "A"	(S) 20
24	XN512-6	C.D. TRIG. TO S.R. "B"	(W-G)	49	XDS 502-2	-85V "A"	(W-BK)
25				50	GND. LUG.	CHASSIS GND	BK

TJ501							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	S506A-1	SHIFT TO DCC	Y	26			
2	S506F-W	RELAY DRIVE	BL	27			
3	S506D-1	S&R FROM DCC	G	28			
4	S506E-1	DATA FROM DCC	(W-BL)	29			
5	S503-NO	RESET TO MONITOR	Y	30			
6	S506D-W	S.R TO DETECTORS	(W-O)	31	XN501-7	TEST SELECT & READY	(W-G)
7				32			
8	S516E-W	DATA TO DETECTORS	(W-G)	33			
9				34	XDS501-2	-85V "B"	(W-S)
10	XN510-3	SHIFT TRIG. TO DET. "A"	(W-O)	35	XN512-8	-20V "B"	S
11	XK501-6	SHIFT FROM DET. "B"	(W-G)	36			
12	XK501-7	SHIFT FROM DET. "A"	(W-Y)	37	TF501-S	0V "B"	BK
13	XN510-6	SHIFT TRIG. TO DET. "B"	Y	38			
14				39	TP 28	+12V "B"	R
15				40	TP 21	-3.5V "B"	(W-V)
16				41	CR509(+)	-10V "A"	V
17				42	TP 2	-3.5V "A"	(W-V)
18	TP 20	-10V "B"	V	43	XN508-1	-15V "A"	(W-S)
19	XN505-1	-15V "B"	(W-S)	44	TP1	+10V "A"	R
20				45	TF502-S	0V "A"	BK
21	XN511-3	SAMPLE TO DET. "A"	(W-BL)	46			
22	XN511-6	SAMPLE TO DET. "B"	W	47	XN512-1	-20V "A"	S
23	XN512-3	C.D. TRIG. TO S.R. "A"	G	48			
24	XN512-6	C.D. TRIG. TO S.R. "B"	(W-G)	49	XDS502-2	-85V "A"	(W-BK)
25				50			

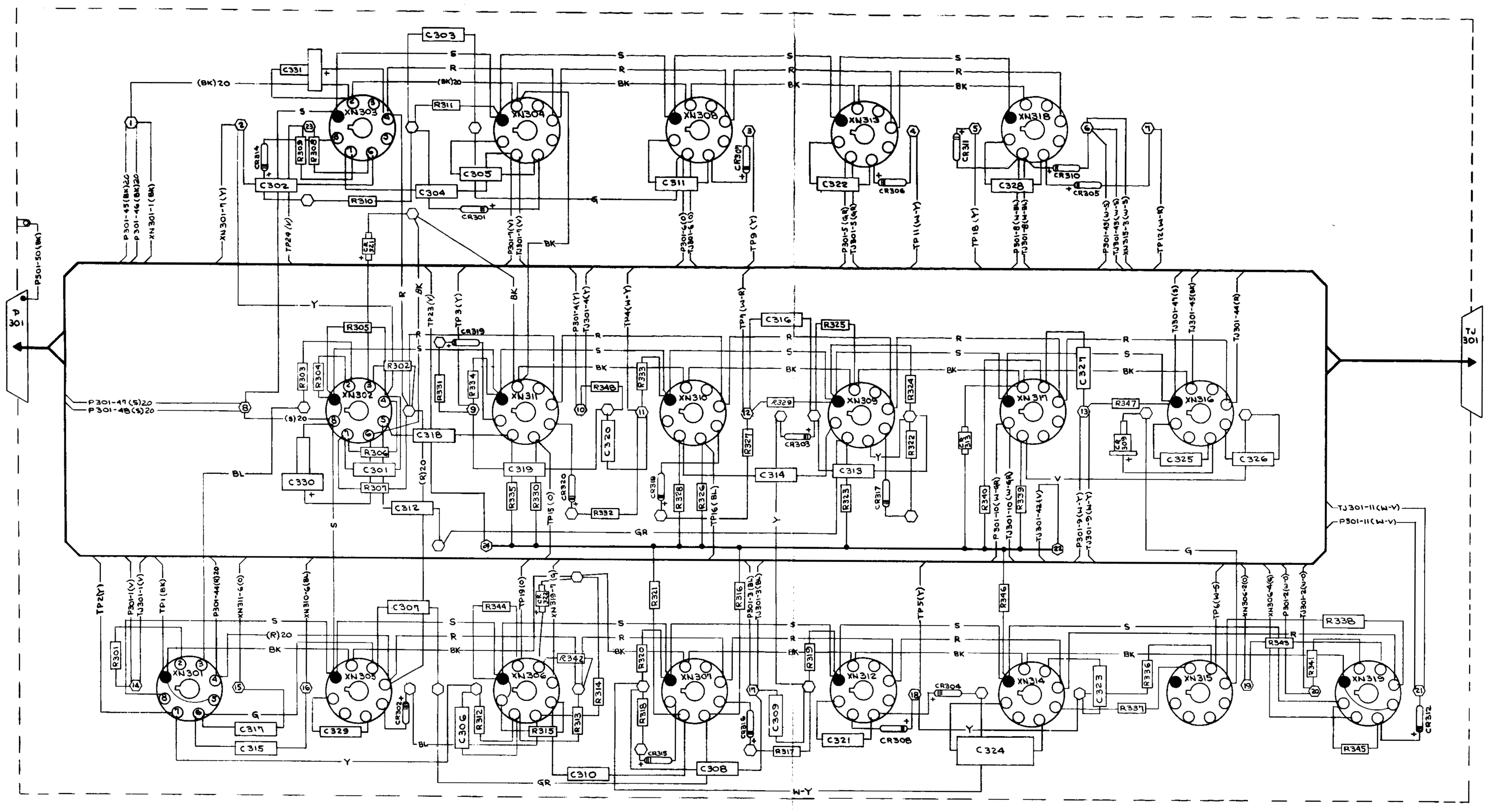
NOTES:
1. --- DENOTES A C LEADS
2. TWIST A C LEADS IN PAIRS
3. ALL WIRE #22 GA. UNLESS OTHERWISE NOTED
4. DO NOT LACE JUMPERS.
5. XK502 SOCKET MOUNTED ON BRACKET LOCATED ON REVERSE SIDE OF CHASSIS

Figure 9-4. Wiring Diagram
Test Control Chassis
Dwg. D74W5A, Sheet 2



NOTES:
1. ALL RESISTORS ½W, ±10% UNLESS SPECIFIED.
2. ALL DIODES CTP-503 OR T12G UNLESS SPECIFIED.

Figure 9-5. Schematic
Detector A Chassis
Dwg. D74S3A



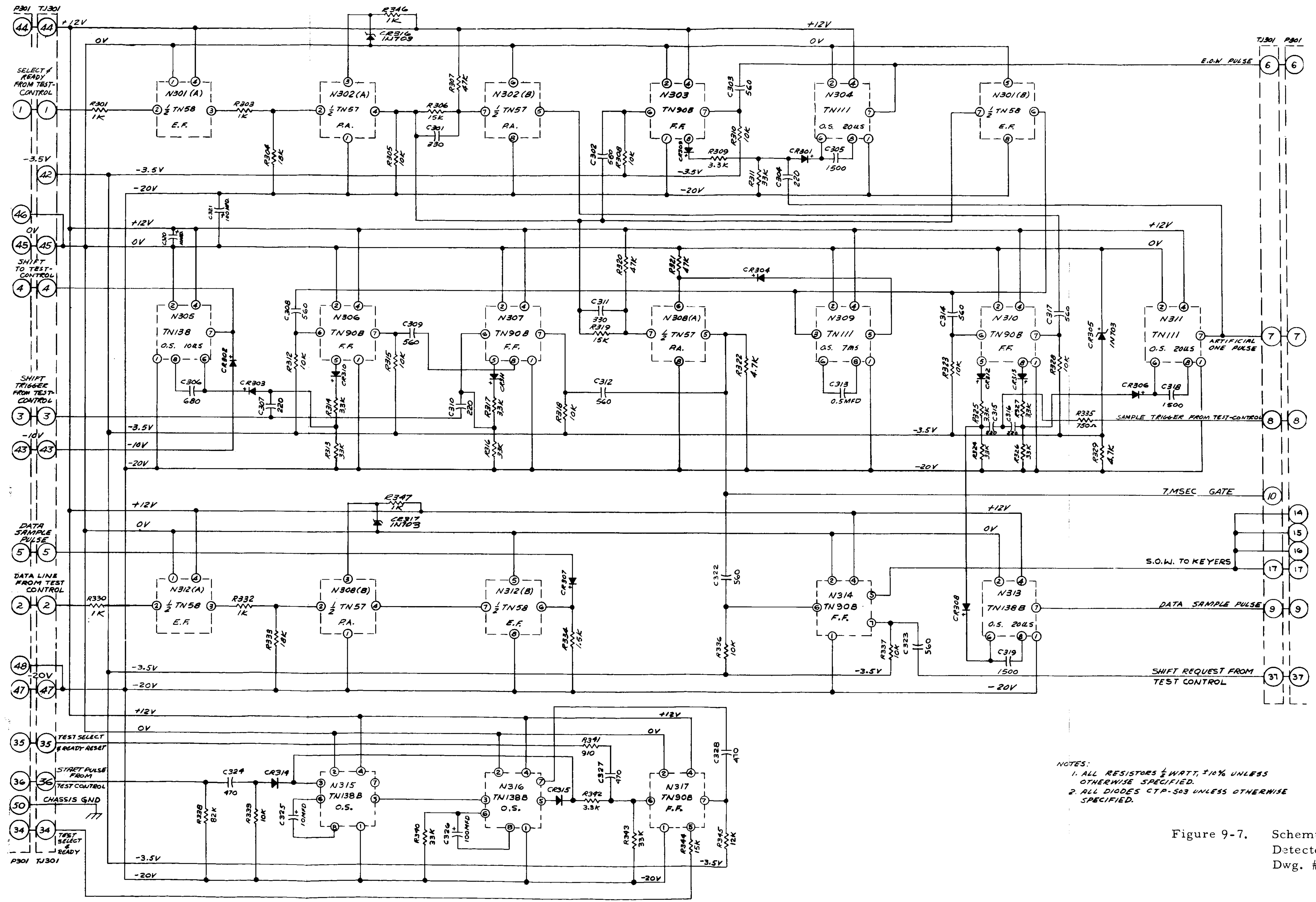
P301							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	TP14	SELECT & READY	V	26			
2	TP20	DATA LINE	W-O	27			
3	TP17	SHIFT TRIGGER	BL	28			
4	TP10	SAMPLE TRIGGER	Y	29			
5	XN313-7	DATA SAMPLE PULSE	GR	30			
6	XN308-7	ARTIFICIAL ONE PULSE	O	31			
7	XN304-7	EOW PULSE	V	32			
8	XN318-7	SHIFT TO TEST CONTROL	W-BL	33			
9	TP13	RESET FROM TEST CONTROL	W-Y	34			
10	XN317-8	RELAY DRIVE LEVEL	W-GR	35			
11	TP21	DATA SAMPLE PULSE	W-V	36			
12				37			
13				38			
14				39			
15				40			
16				41			
17				42			
18				43	TP6	-10V	W-S
19				44	XN301-4	+12V	(R)20
20				45	TP1	0V	BK
21				46	TP1	0V	BK
22				47	TP8	-20V	S
23				48	TP8	-20V	S
24				49			
25				50	GND LUG	CHASSIS GND	BK

TJ301							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	TP14	SELECT & READY	V	26			
2	TP20	DATA LINE	W-O	27			
3	TP17	SHIFT TRIGGER	BL	28			
4	TP10	SAMPLE TRIGGER	Y	29			
5	XN313-7	DATA SAMPLE PULSE	GR	30			
6	XN308-7	ARTIFICIAL ONE PULSE	O	31			
7	XN304-7	EOW PULSE	V	32			
8	XN318-7	SHIFT TO TEST CONTROL	W-BL	33			
9	TP13	RESET FROM TEST CONTROL	W-Y	34			
10	XN317-8	RELAY DRIVE LEVEL	W-GR	35			
11	TP21	DATA SAMPLE PULSE	W-V	36			
12				37			
13				38			
14				39			
15				40			
16				41			
17				42	TP22	-3.5V	V
18				43	TP-6	-10V	W-S
19				44	XN316-4	+12V	R
20				45	XN316-2	0V	BK
21				46			
22				47	XN316-1	-20V	S
23				48			
24				49			
25				50			

NOTES

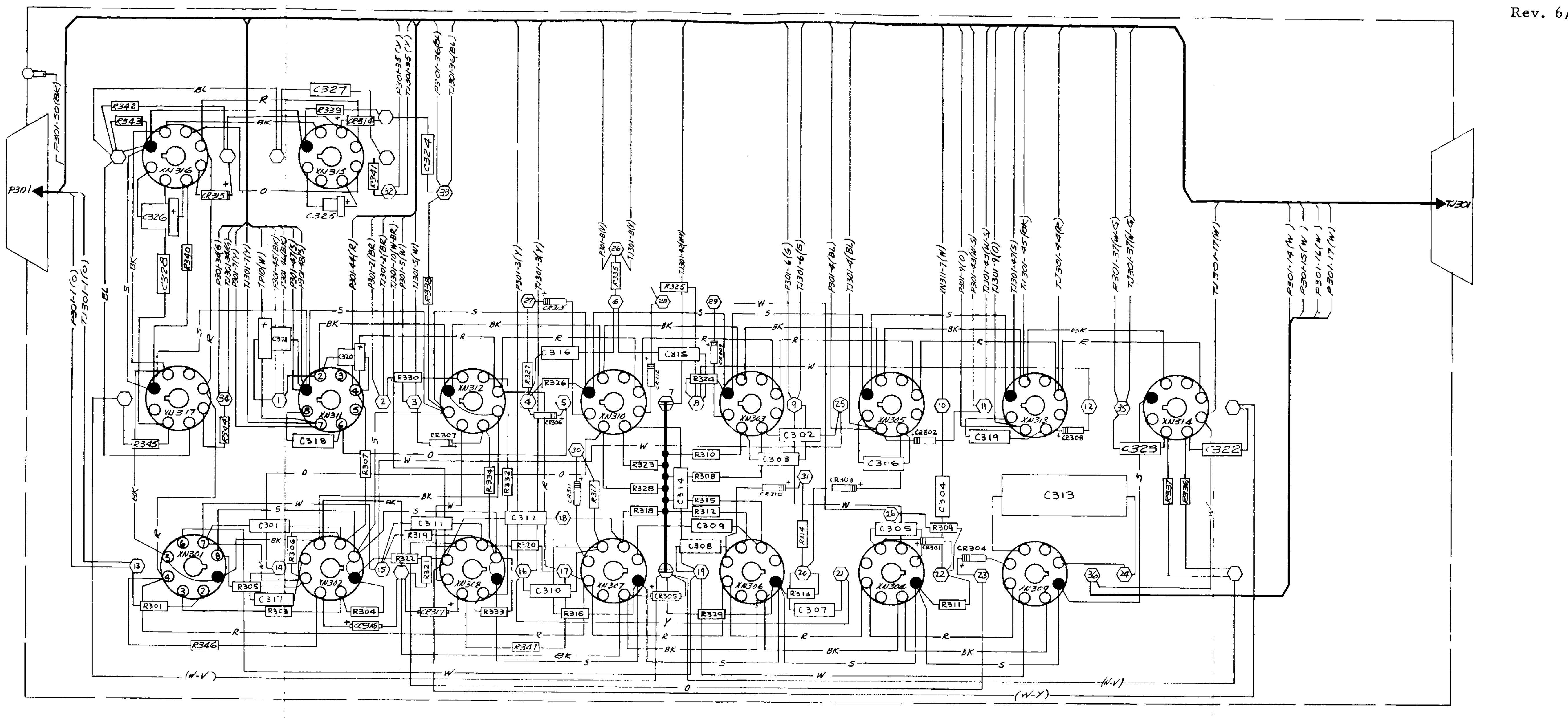
1- ALL WIRE TO BE #22 GA. UNLESS OTHERWISE SPECIFY

Figure 9-6. Wiring Diagram Detector A Chassis Dwg. #D74W3A



NOTES:
1. ALL RESISTORS ½ WATT, ±10% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES CTP-503 UNLESS OTHERWISE SPECIFIED.

Figure 9-7. Schematic Detector B Chassis Dwg. #D74S3B



P301

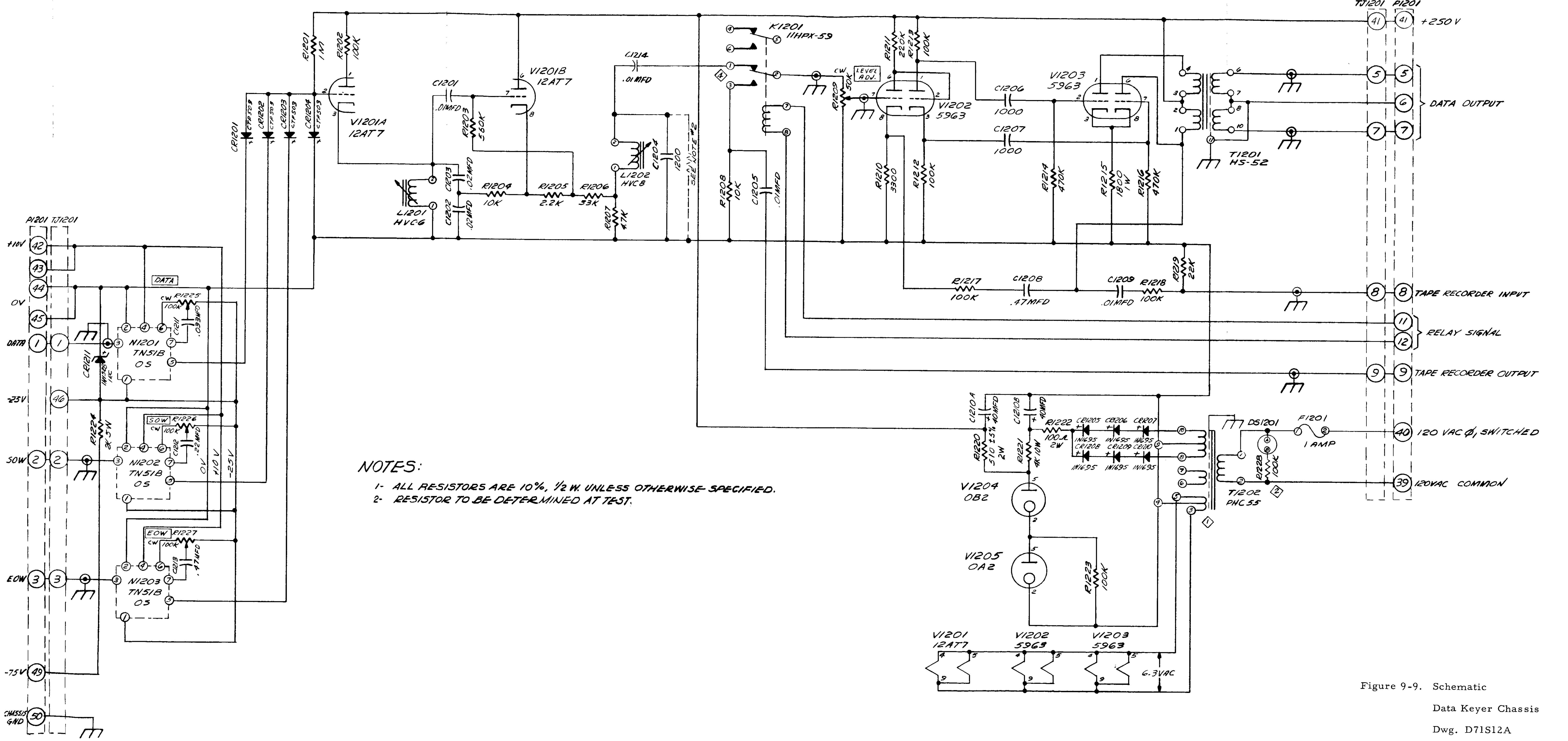
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	TP13	SELECT & READY FROM TEST CNTL	O	26			
2	TP2	DATA LINE FROM TEST CONTROL	BR	27			
3	TP16	SHIFT TRIGGER FROM TEST CONTROL	Y	28			
4	XN305-7	SHIFT TO TEST CONTROL	BL	29			
5	TP3	DATA SAMPLE PULSE	W	30			
6	TP9	E.O.W. PULSE	G	31			
7	XN311-7	ARTIFICIAL ONE PULSE	Y	32			
8	TP6	SAMPLE TRIG. FROM TEST CONTROL	V	33			
9	XN313-7	DATA SAMPLE PULSE	O	34	TP 34	TEST SELECT & READY	G
10				35	TP 32	TEST SELECT & READY RESET	Y
11				36	TP 33	START PULSE FROM TEST CNTL	BL
12				37	TP 35	SHIFT REQ. FROM TEST CNTL	W-G
13				38			
14	TP 36	S.O.W. TO KEYERS	W	39			
15	TP 36	" " "	W	40			
16	TP 36	" " "	W	41			
17	TP 36	" " "	W	42			
18				43	TP11	-10 V	W-S
19				44	XN311-4	+12 V	R
20				45	TP1	0 V	BK
21				46	TP1	0 V	BK
22				47	XN311-1	-20 V	S
23				48	XN311-1	-20 V	S
24				49			
25				50	CHASSIS GN'D.		BK

TJ301

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	TP13	SELECT & READY FROM TEST CNTL.	O	26			
2	TP2	DATA LINE FROM TEST CONTROL	BR	27			
3	TP16	SHIFT TRIGGER FROM TEST CONTROL	Y	28			
4	XN305-7	SHIFT TO TEST CONTROL	BL	29			
5	TP3	DATA SAMPLE PULSE	W	30			
6	TP9	E.O.W. PULSE	G	31			
7	XN311-7	ARTIFICIAL ONE PULSE	Y	32			
8	TP6	SAMPLE TRIG. FROM TEST CONTROL	V	33			
9	XN313-7	DATA SAMPLE PULSE	O	34	TP 34	TEST SELECT & READY	G
10	XN308-5	1 M SEC. GATE	W-BR	35	TP 32	TEST SELECT & READY RESET	Y
11				36	TP 33	START PULSE FROM TEST CNTL.	BL
12				37	TP 35	SHIFT REQ. FROM TEST CNTL.	W-G
13				38			
14				39			
15				40			
16				41			
17	XN314-5	S.O.W. TO KEYERS	W	42	TP7	-3.5 V	W-V
18				43	TP11	-10 V	W-S
19				44	XN313-4	+12 V	R
20				45	XN313-2	0 V	BK
21				46			
22				47	XN313-1	-20 V	S
23				48			
24				49			
25				50			

NOTES:
1. ALL WIRES TO BE #22GA UNLESS SPECIFIED

Figure 9-8. Wiring Diagram
Detector B Chassis
Dwg. D74W3B



NOTES:

1- ALL RESISTORS ARE 10%, 1/2 W. UNLESS OTHERWISE SPECIFIED.

2- RESISTOR TO BE DETERMINED AT TEST.

Figure 9-9. Schematic
Data Keyer Chassis
Dwg. D71S12A

P1201

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN1201-3	DATA	COAX	26			
2	XN1202-3	SOW	COAX	27			
3	XN1203-3	EOW	COAX	28			
4				29			
5	T1201-6	DATA OUTPUT	COAX	30			
6	T1201-8	DATA OUTPUT	W-V	31			
7	T1201-10	DATA OUTPUT	COAX	32			
8	TP-6	TAPE RECORDER INPUT	COAX	33			
9	TP-5	TAPE RECORDER OUTPUT	COAX	34			
10				35			
11	K1201-7	RELAY SIGNAL	W-R	36			
12	K1201-8	RELAY SIGNAL	W-G	37			
13				38			
14				39	T1202-2	120VAC COMMON	W
15				40	XF1201-2	120VAC Ø, SWITCHED	S
16				41	TP14 ⑤	+250V	R
17				42	XN1201-4	+10V	W-R
18				43	XN1203-4	+10V	W-R
19				44	XN1201-2	0V	BK
20				45	XN1203-2	0V	BK
21				46			
22				47			
23				48			
24				49	TP-1	-75V	W-S
25				50	GND LUG	CHASSIS GND	BK

TJ1201

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN1201-3	DATA	COAX	26			
2	XN1202-3	SOW	COAX	27			
3	XN1203-3	EOW	COAX	28			
4				29			
5	T1201-6	DATA OUTPUT	COAX	30			
6				31			
7	T1201-10	DATA OUTPUT	COAX	32			
8	TP-6	TAPE RECORDER INPUT	COAX	33			
9	TP-5	TAPE RECORDER OUTPUT	COAX	34			
10				35			
11				36			
12				37			
13				38			
14				39			
15				40			
16				41	XC1210-3	+250V	R
17				42			
18				43			
19				44			
20				45			
21				46	XN1201-1	-75V	W-BK
22				47			
23				48			
24				49			
25				50			

NOTES:
1. INDICATES COAX RG174/U
2. (1) INDICATES TIE-POINT
3. ALL WIRE TO BE #22GA. UNLESS OTHERWISE SPECIFIED.
4. GROUND ONE END ONLY OF ALL COAX SHIELDS.
5. GROUND ALL CENTER POSTS OF TUBE SOCKETS
6. TWIST ALL FILAMENT WIRES
7. GROUND TO CHASSIS T1201-11

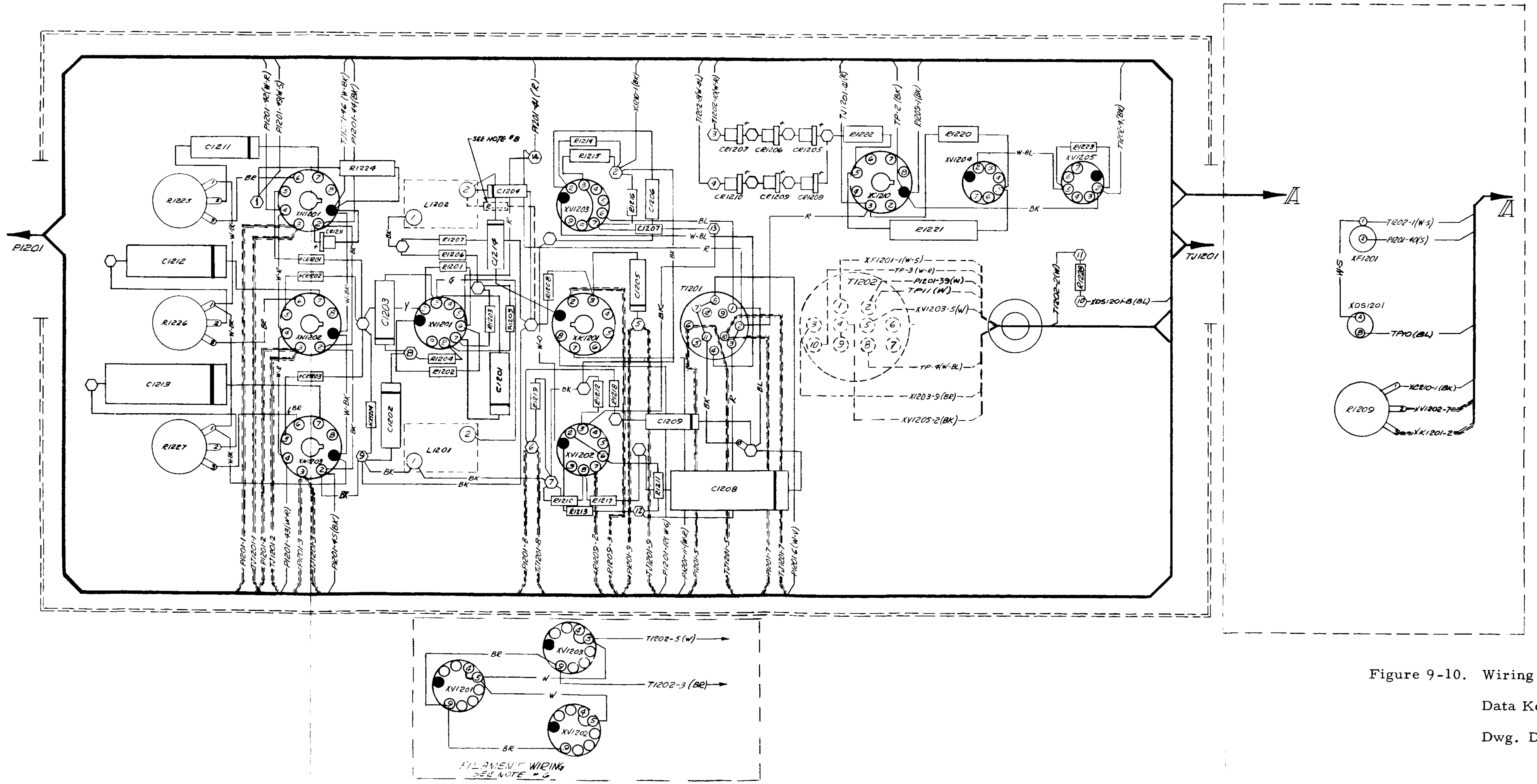


Figure 9-10. Wiring Diagram
Data Keyer Chassis
Dwg. D71W12A

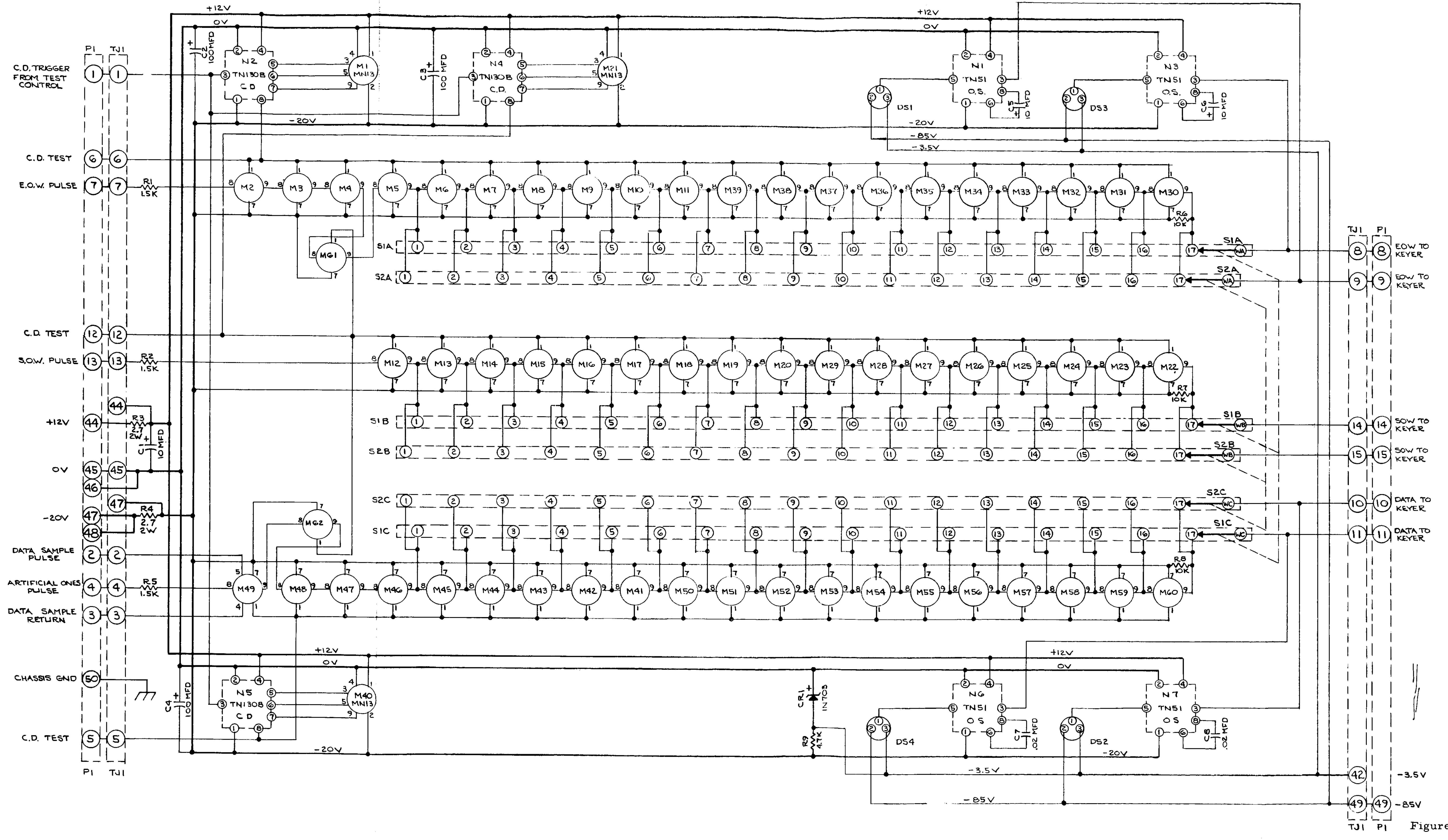
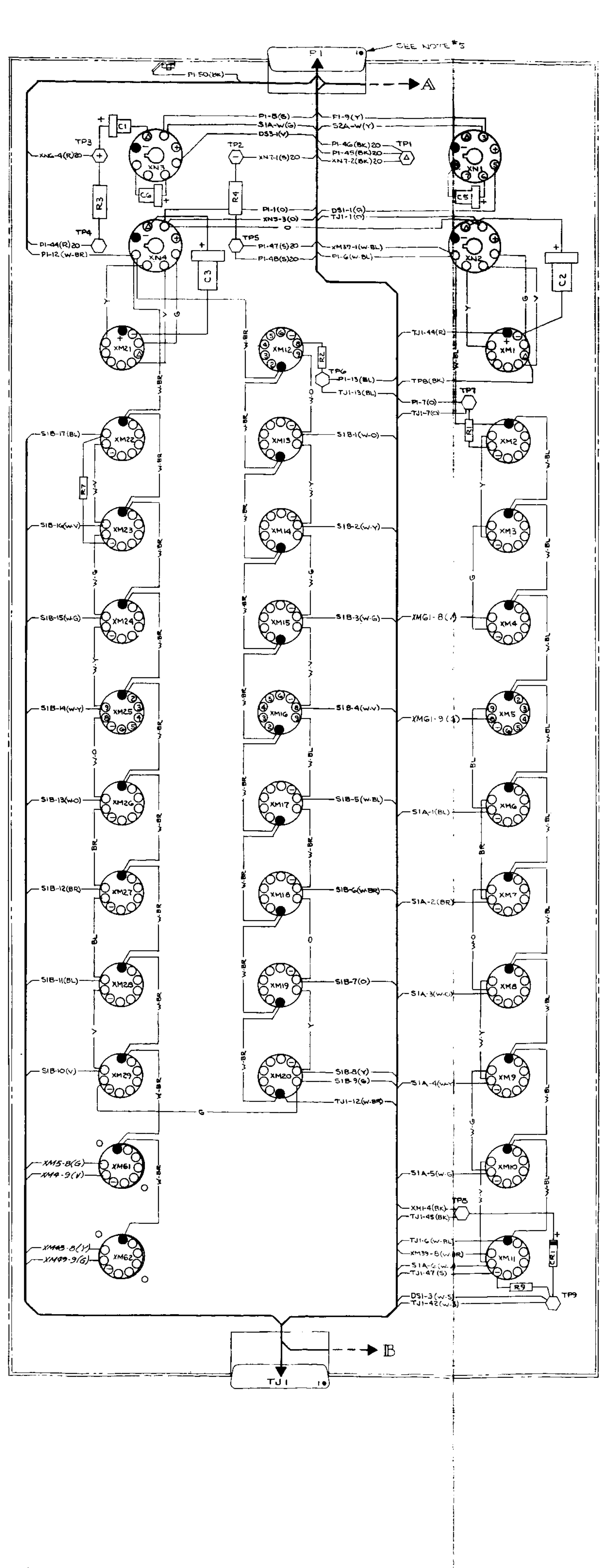


Figure 9-11. Schematic, Variable Delay Shift Register (D7458A/2)

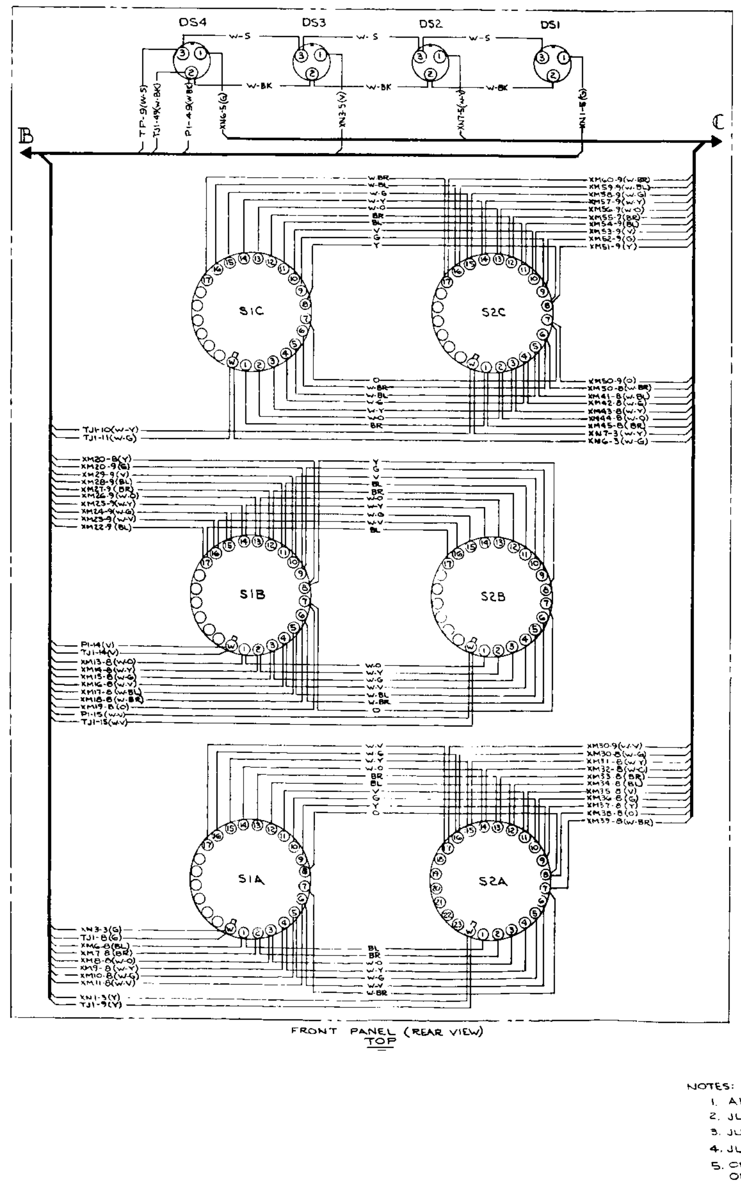
NOTES:

1. ALL CORES MN11 UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS 1/2 W, ±10% UNLESS OTHERWISE SPECIFIED.
3. ALL INDICATORS MEC # 16-102

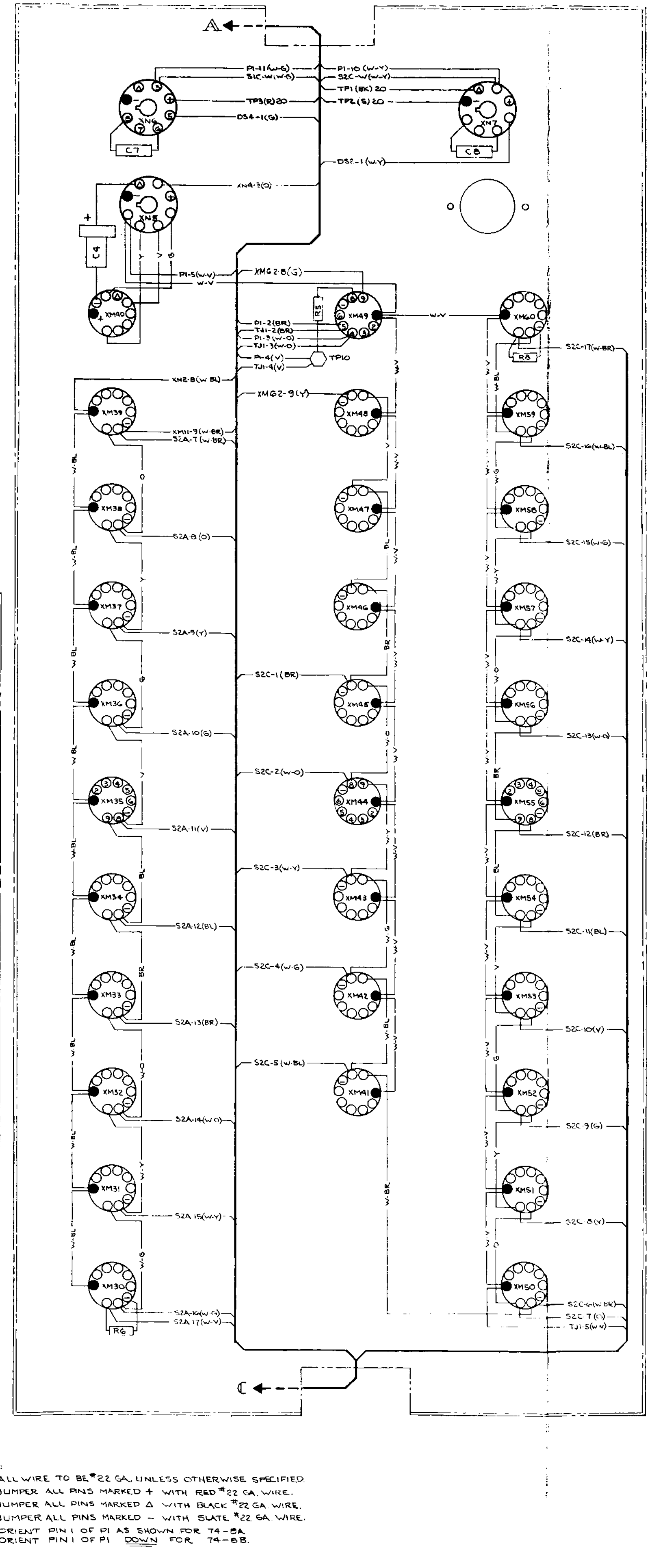


P1							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN4-3	C.D. TRIGGER	O	26			
2	XM49-5	DATA SAMPLE PULSE	BR	27			
3	XM49-4	DATA SAMPLE RETURN	W-O	28			
4	TP10	ARTIFICIAL ONES	Y	29			
5	XN5-8	C.D. TEST	W-Y	30			
6	XN2-8	C.D. TEST	W-BL	31			
7	TP7	E.O.W. PULSE	O	32			
8	XN3-3	E.O.W. TO KEYER	G	33			
9	XN1-3	E.O.W. TO KEYER	Y	34			
10	XN7-3	DATA TO KEYER	W-Y	35			
11	XN6-3	DATA TO KEYER	W-G	36			
12	XN4-8	C.D. TEST	W-BR	37			
13	TP6	S.O.W. PULSE	BL	38			
14	S1B-W	S.O.W. TO KEYER	V	39			
15	S2B-W	S.O.W. TO KEYER	W-V	40			
16				41			
17				42			
18				43			
19				44	TP4	+12V	(R)#20
20				45	TP1	0V	(BK)#20
21				46	TP1	0V	(BK)#20
22				47	TP5	-20V	(S)#20
23				48	TP5	-20V	(S)#20
24				49	DS1-2	-85V	W-BK
25				50	GND LUG	CHASSIS GND	BK

TJ1							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN2-3	C.D. TRIGGER	O	26			
2	XM49-5	DATA SAMPLE PULSE	BR	27			
3	XM49-4	DATA SAMPLE RETURN	W-O	28			
4	TP10	ARTIFICIAL ONES	Y	29			
5	XM50-1	C.D. TEST	W-Y	30			
6	XM11-1	C.D. TEST	W-BL	31			
7	TP7	E.O.W. PULSE	O	32			
8	S1A-W	E.O.W. TO KEYER	G	33			
9	S2A-W	E.O.W. TO KEYER	Y	34			
10	S2C-W	DATA TO KEYER	W-Y	35			
11	S1C-W	DATA TO KEYER	W-G	36			
12	XM20-1	C.D. TEST	W-BR	37			
13	TP6	S.O.W. PULSE	BL	38			
14	S1B-W	S.O.W. TO KEYER	V	39			
15	S2B-W	S.O.W. TO KEYER	W-V	40			
16				41			
17				42	TP9	-3.5V	W-S
18				43			
19				44	XM1-1	+12V	R
20				45	TP8	0V	BK
21				46			
22				47	XM11-7	-20V	S
23				48			
24				49	DS1-2	-85V	W-BK
25				50			

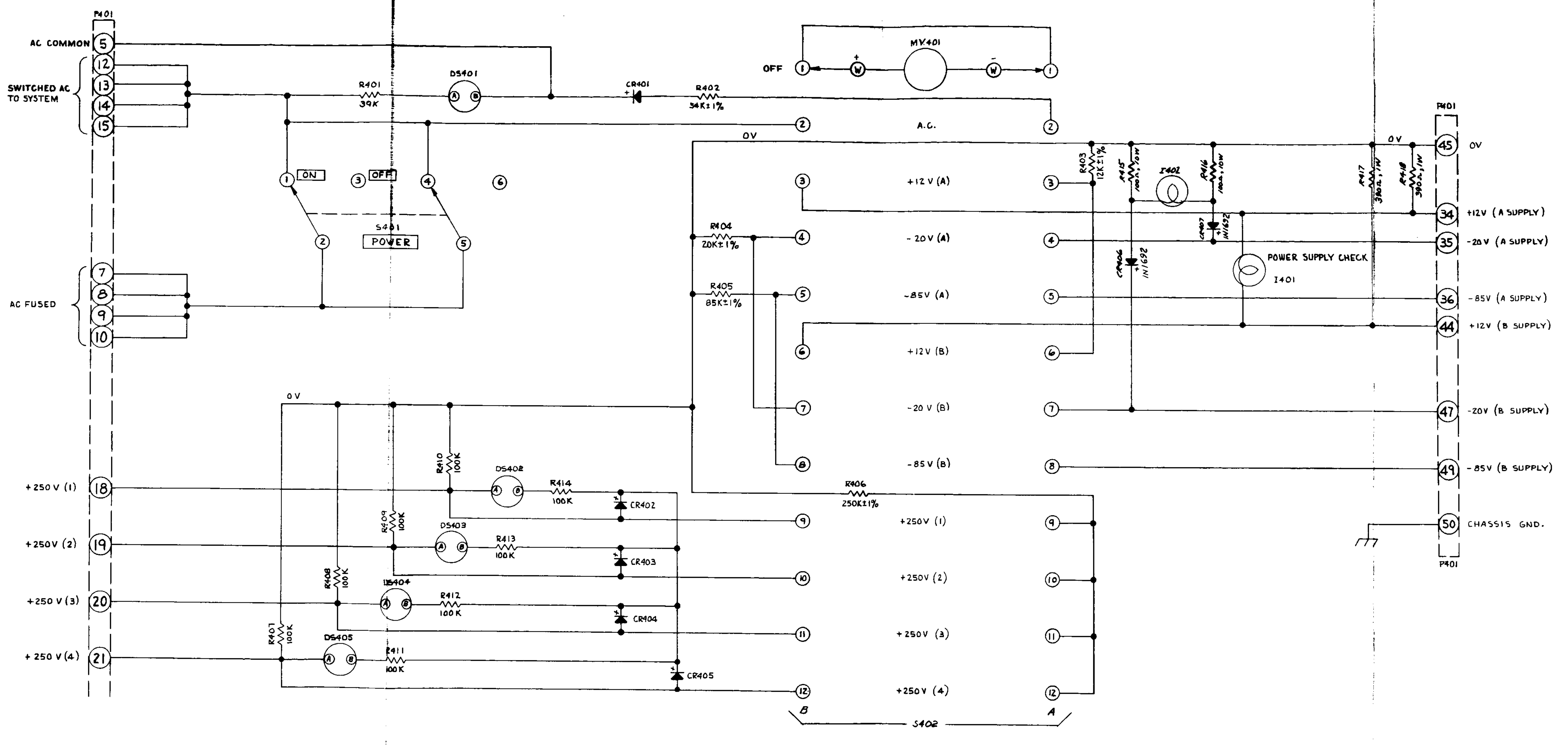


FRONT PANEL (REAR VIEW)
TOP



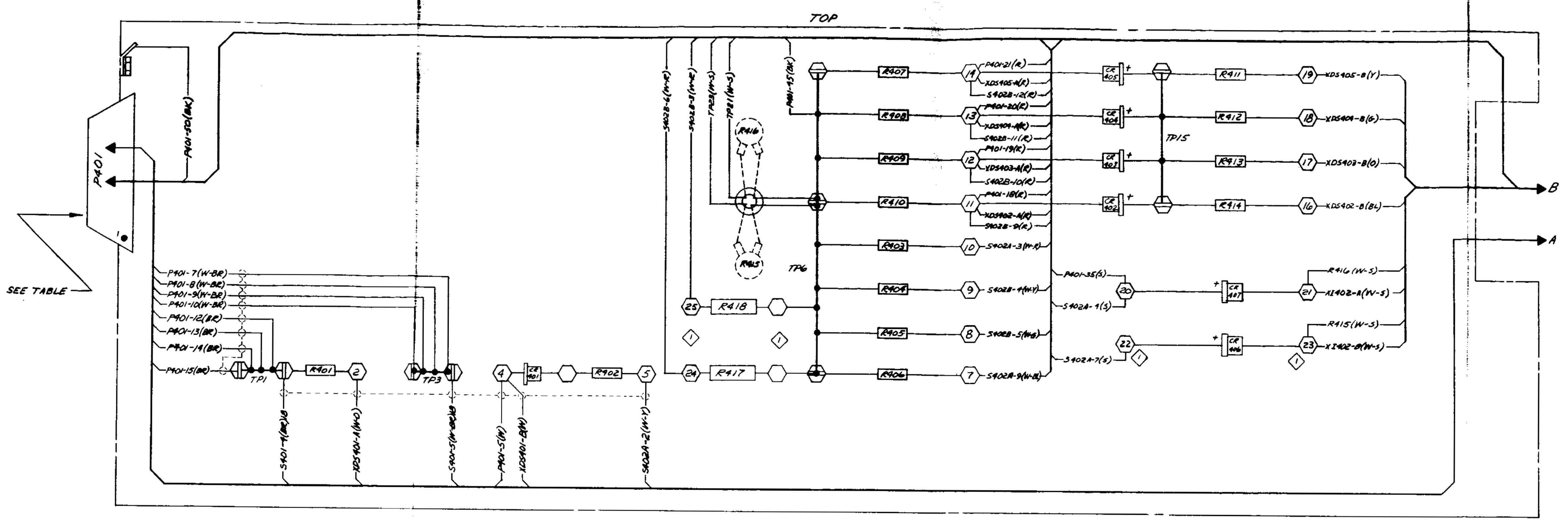
NOTES:
1. ALL WIRE TO BE #22 GA. UNLESS OTHERWISE SPECIFIED.
2. JUMPER ALL PINS MARKED + WITH RED #22 GA. WIRE.
3. JUMPER ALL PINS MARKED Δ WITH BLACK #22 GA. WIRE.
4. JUMPER ALL PINS MARKED – WITH SLATE #22 GA. WIRE.
5. ORIENT PIN 1 OF P1 AS SHOWN FOR 74-8A.
ORIENT PIN 1 OF P1 DOWN FOR 74-8B.

Figure 9-12. Wiring Diagram, Variable Delay Shift Register (E74W8A/2)

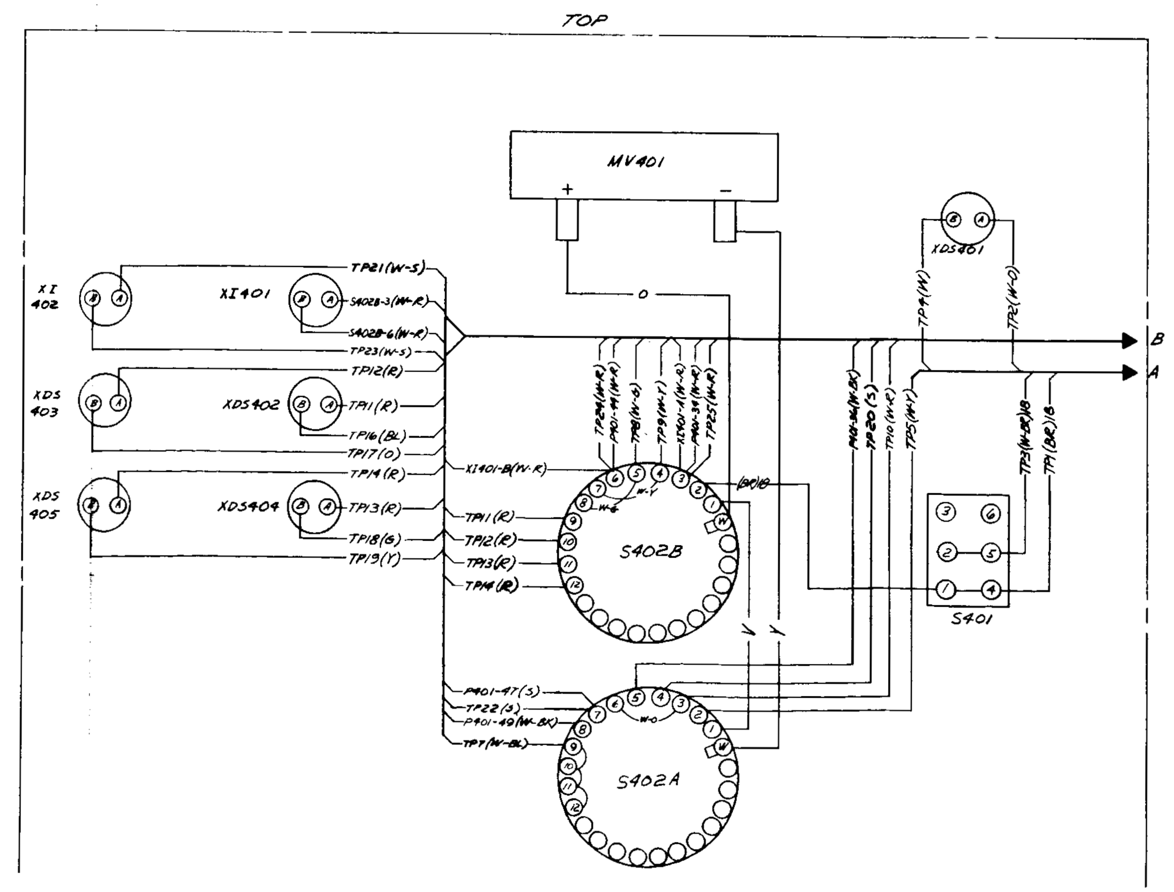


NOTES:
1. ALL DIODES IN1695 UNLESS SPECIFIED.
2. ALL RESISTORS ±10%, 1/4 W, UNLESS SPECIFIED.

Figure 9-13. Schematic Power Control Chassis Dwg. #D74S4A

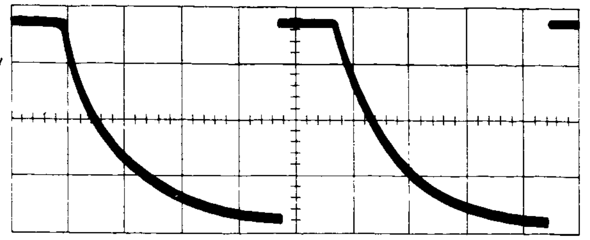


NOTES:
1. ◇-◇ DENOTES TWISTED LEADS.
2. S402A DECK NEAREST FRONT PANEL
3. ALL WIRE #22 GA. UNLESS NOTED.

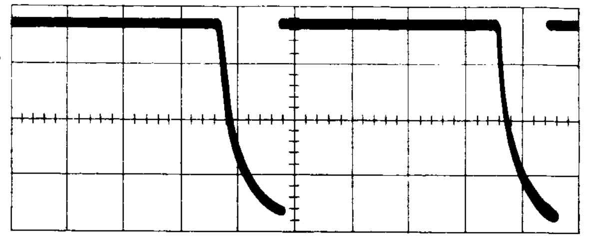


P401							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1				26			
2				27			
3				28			
4				29			
5	TP4	AC COMMON	W	30			
6				31			
7	TP3	AC FUSED	W-BR	32			
8				33			
9				34	S402B-3	+12 (A SUPPLY)	W-R
10	TP3	AC FUSED	W-BR	35	TP20	-20V (A SUPPLY)	S
11				36	S402A-5	-85V (A SUPPLY)	W-BK
12	TP1	SWITCHED AC TO SYSTEM	BR	37			
13				38			
14				39			
15	TP1	SWITCHED AC TO SYSTEM	BK	40			
16				41			
17				42			
18	TP11	+250 (1)	R	43			
19	TP12	+250 (2)	R	44	S402B-6	+12V (B SUPPLY)	W-R
20	TP13	+250 (3)	R	45	TP6	OV	BK
21	TP14	+250 (4)	R	46			
22				47	S402A-7	-20V (B SUPPLY)	S
23				48			
24				49	S402A-8	-85V (B SUPPLY)	W-BK
25				50	GND. LUG	CHASSIS GND	BK

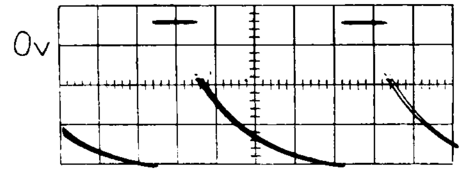
Figure 9-14. Wiring Diagram
Power Control Chassis
Dwg. #D74W4A



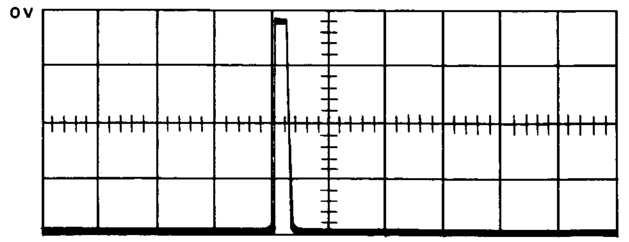
a. **Shift Trigger to Detector**
5v/division and 0.2 MSec/division



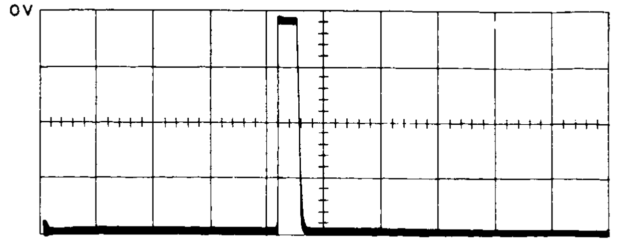
b. Sample Trigger to Detector
5v/division and 0.2 MSec/division



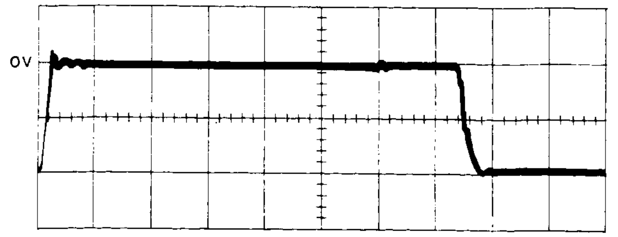
c. Core Driver Trigger to S. R.
5v/division and 0.2 MSec/division



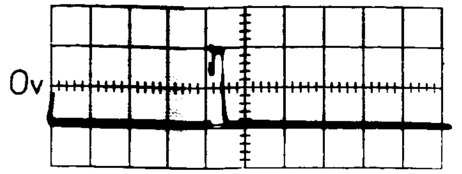
d. Artificial "1" Pulse to S. R.
5v/division and 50 microsec/division



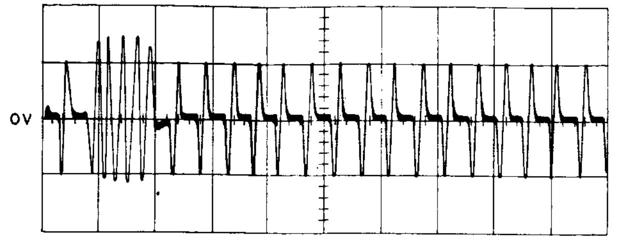
e. Data Sample Pulse to S. R.
5v/division and 50 microsec/division



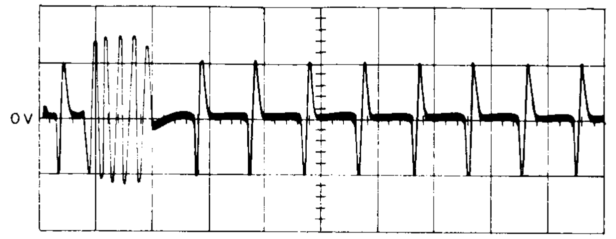
f. Shift Request Pulse to Test-Control
5v/division and 1 microsec/division



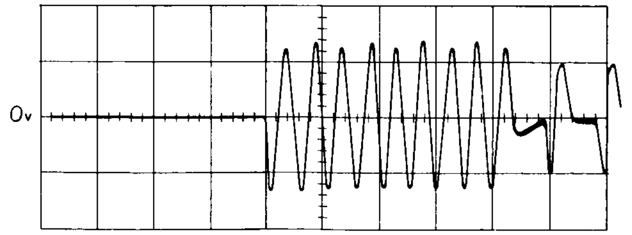
g. Output Keyer - all "0"s followed by EOW, artificial "1"s and SOW
.1 sec/division



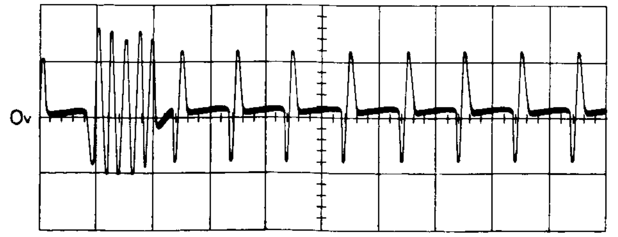
h. Keyer Output - artificial "1"s, SOW, all "1"s test pattern
2 MSec/division



i. Keyer Output - artificial "1"s, SOW, alternate "1"s and "0"s test pattern
2 MSec/division



j. Keyer Output - all "0"s, EOW, artificial "1"s
1 MSec/division



k. Complete Word
100 MSec/division

Figure 9-15. Waveforms

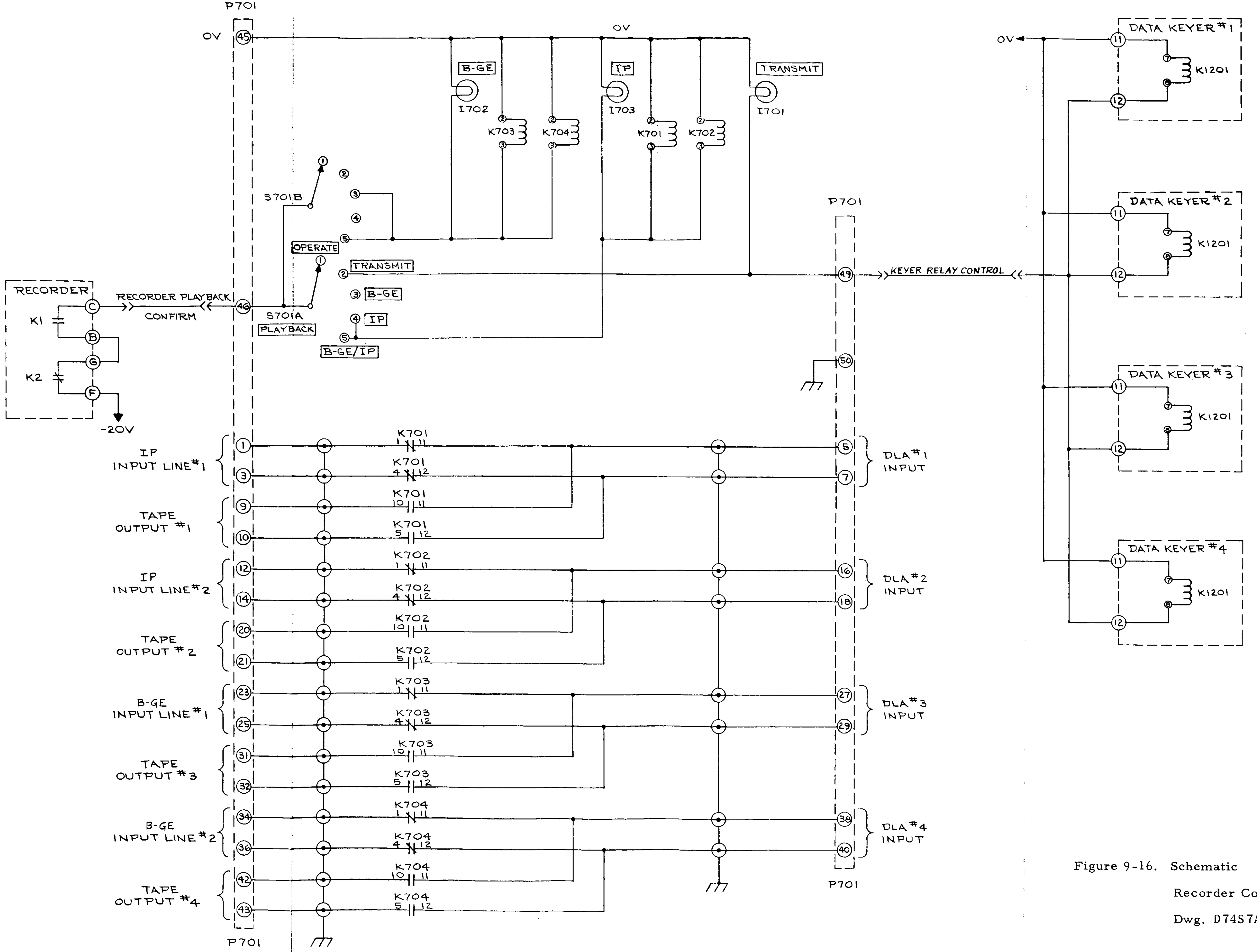
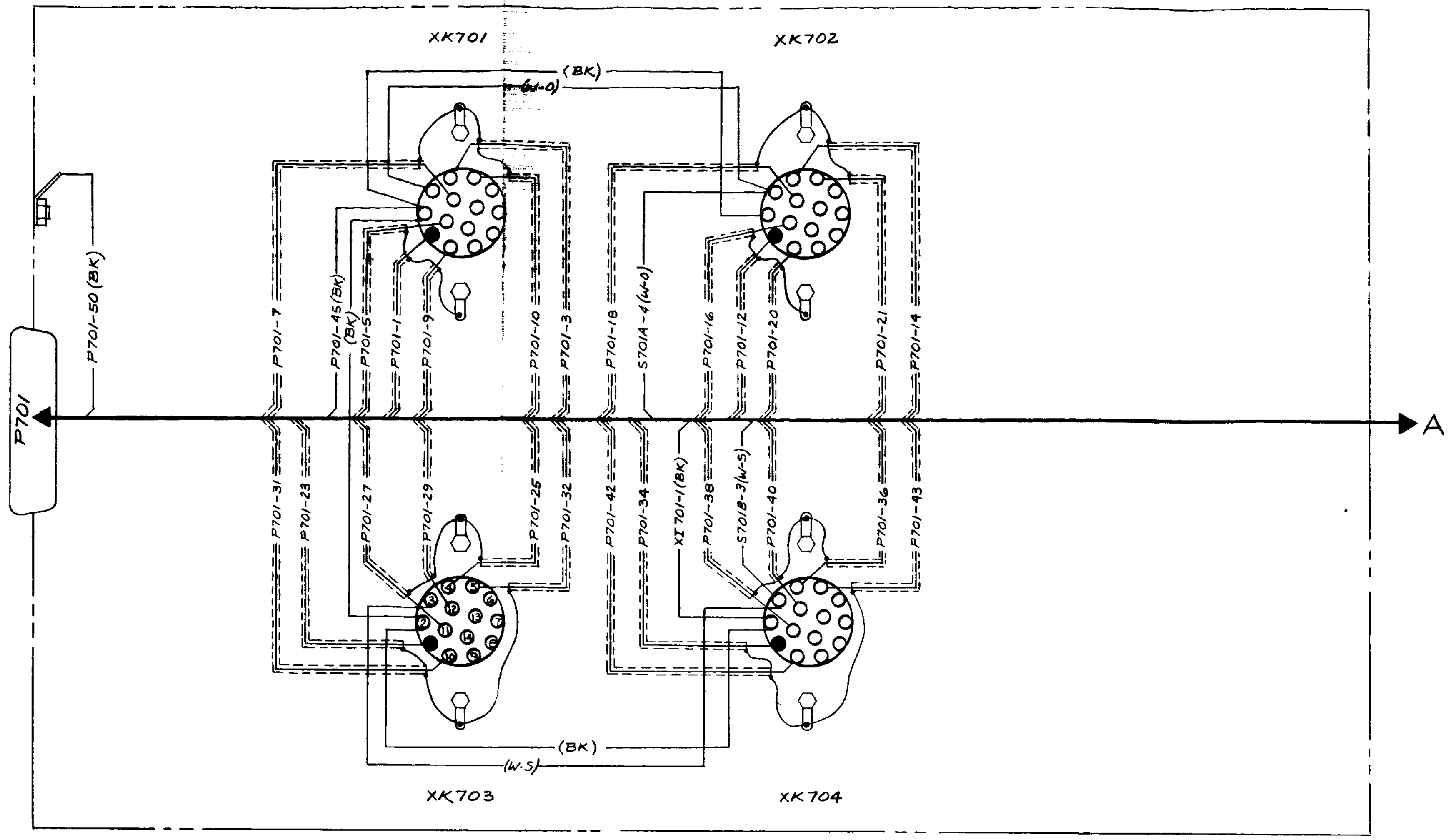
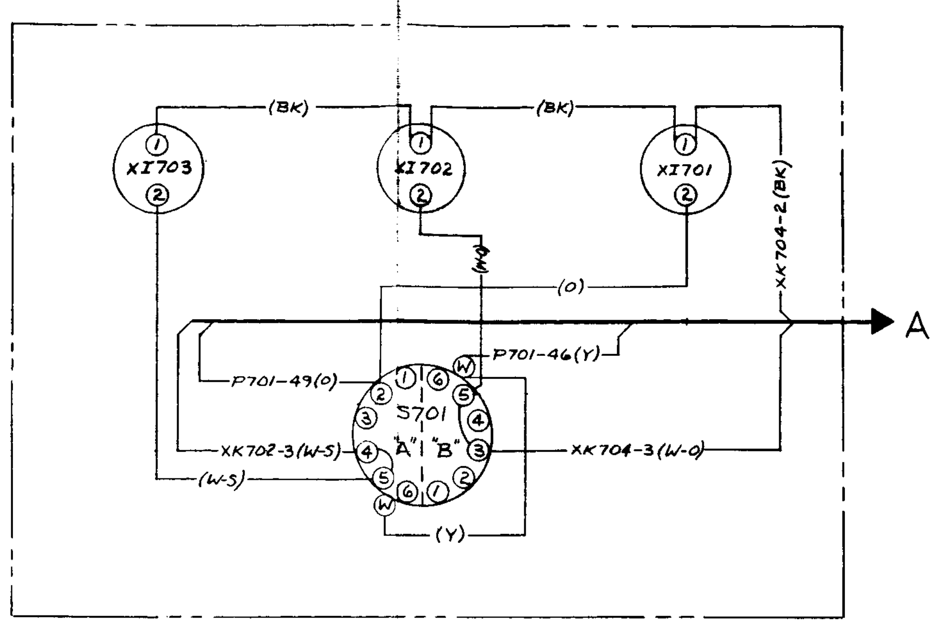


Figure 9-16. Schematic
Recorder Control Chassis
Dwg. D74S7A



TOP



REAR OF FRONT PANEL

P701							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XK701-1	IP INPUT LINE #1	COAX	26			
2				27	XK703-11	DLA #3 INPUT	COAX
3	XK701-4	IP INPUT LINE #1	COAX	28			
4				29	XK703-12	DLA #3 INPUT	COAX
5	XK701-11	DLA #1 INPUT	COAX	30			
6				31	XK703-10	TAPE OUTPUT #3	COAX
7	XK701-12	DLA #1 INPUT	COAX	32	XK703-5	TAPE OUTPUT #3	COAX
8				33			
9	XK701-10	TAPE OUTPUT #1	COAX	34	XK704-1	B-6E INPUT LINE #2	COAX
10	XK701-5	TAPE OUTPUT #1	COAX	35			
11				36	XK704-4	B-6E INPUT LINE #2	COAX
12	XK702-1	IP INPUT LINE #2	COAX	37			
13				38	XK704-11	DLA #4 INPUT	COAX
14	XK702-4	IP INPUT LINE #2	COAX	39			
15				40	XK704-12	DLA #4 INPUT	COAX
16	XK702-11	DLA #2 INPUT	COAX	41			
17				42	XK704-10	TAPE OUTPUT #4	COAX
18	XK702-12	DLA #2 INPUT	COAX	43	XK704-5	TAPE OUTPUT #4	COAX
19				44			
20	XK702-10	TAPE OUTPUT #2	COAX	45	XK701-2	OV	BK
21	XK702-5	TAPE OUTPUT #2	COAX	46	S701B-W	RECORDER PLAYBACK CONFIRM	Y
22				47			
23	XK703-1	B-6E INPUT LINE #1	COAX	48			
24				49	S701A-2	KEYER RELAY CONTROL	O
25	XK703-4	B-6E INPUT LINE #1	COAX	50	GND LUG	CHASSIS GND	BK

NOTES:
1. ALL WIRES ARE #22 GA. UNLESS OTHERWISE SPECIFIED.

Figure 9-17. Wiring Diagram
Recorder Control Chassis
Dwg. D74W7A

ADDENDUM
CHAPTER X

10-1. FOUR CHANNEL TEST DATA KEYER, MEC MODEL 74-9A

10-1.1. Function

10-1.1.1. The Four Channel Test Data Keyer is used to transmit a continuous burst of binary "1"s on any combination of form channels. This unit is installed in the MEC Model 74 Data Transmitter and works in conjunction with it. A schematic of the Test Data Keyer is shown in Figure 10-1. The four Keyer outputs from the Model 74 are wired to the Test Data Keyer Chassis by a jumper cable between the rack output connector, J16, and connector J23 on the Test Data Keyer Chassis. These Keyer outputs are then routed directly through the 74-9A or are disconnected.

10-1.1.2. The Test Data Keyer continuously generates an all "1"s pattern. This output is wired to four switches on the front panel of the Test Data Keyer Chassis, each of which is related to one of the four 71-12A Keyers located in the Model 74 Transmitter rack. When a given switch is placed in the TEST position, the output of the 71-12A Keyer corresponding to that switch is disconnected from the transmission line. The all "1"s output from the Data Keyer Chassis is placed on the line. Since each line operates independently, the output of the Test Data Keyer Chassis may be switched on to any combination of the four transmission lines.

10-1.2. Circuit Analysis

10-1.2.1. Pulses are generated at a 1 kc rate by N1, a TN901 oscillator. The output of N1, a positive-going pulse, drives N2, a TN506B one-shot. When N2 is triggered the pin 10 output goes from -12 volts to 0 volts. The pulse is level shifted by Zener diode CR7 and is used to turn on N3, a 2 kc gated oscillator. The output of N3 goes through a band pass filter, R22, C5 and C6, and drives N4 and N5, two line driver amplifiers. The output of N4 is used for driving lines 1 and 2 (corresponding to Transmitter 1 and 2). The output of N5 drives lines 3 and 4.

10-1.2.2. The frequency of N1 is controlled by two potentiometers, R1 and R20. Potentiometer R1 is the coarse frequency control, R20, the fine control. Since N3 is a gated oscillator, the width of the input pulse determines the output wave form. Potentiometer R2 is a control on the width of N2, so that a proper signal may be generated by N3. The frequency of N3 is determined by the tank circuit, L1 and C1.

10-1.2.3. The outputs of N4 and N5 drive impedance matchine transformers and the two lines each. Each output of the transformers is padded to maintain a minimum of interplay between circuits. When a given switch is placed in the OPERATE position, a dummy load is placed across that output of the Test Data Keyer Chassis to maintain a constant load on the transformer.

10-1.2.4. The Test Data Keyer also has a self-contained power supply which requires 60 and 110 volts ac. This input voltage is brought into the chassis and stepped down in T3. It is then full-wave rectified, filtered and regulated. The regulation is performed by two Zener diodes, CR5 and CR6.

10-1.3. Installation

10-1.3.1. The Test Data Keyer Chassis is installed in the center blank panel of the MEC Model 74 Data Transmitter as follows:

Step 1. Remove the AC power cable from J15, located on the main connector panel of the rack. Connect it to J21 of the Test Data Keyer.

Step 2. Connect the AC jumper from J22 on the Test Data Keyer to J15 Data Keyer.

Step 3. Remove the output data cable from J16, located on the main connector panel of the rack and place it on J24 of the Test Data Keyer.

Step 4. Connect the output data jumper cable from J16 of the rack connector panel to J23 of the Test Data Keyer.

10-1.4. Adjustments

10-1.4.1. The main power for the Model 74 Data Transmitter rack operates independently of the AC power switch on the Test Data Keyer.

Step 1. Place the AC power switch located on the front panel of the Test Data Keyer in the ON position.

Step 2. Allow 30 minutes for warmup.

Step 3. Place an ungrounded oscilloscope and a EPUT Meter on TJ1 and TJ2.

Step 4. Place all control switches in the TEST position. If there is no signal on the oscilloscope, rotate R3 until one appears.

Step 5. Remove N2.

Step 6. Adjust L1 until a 2 kc sine wave appears on the oscilloscope.

Step 7. Adjust R3 until the output is the desired amplitude.

Step 8. Replace N2.

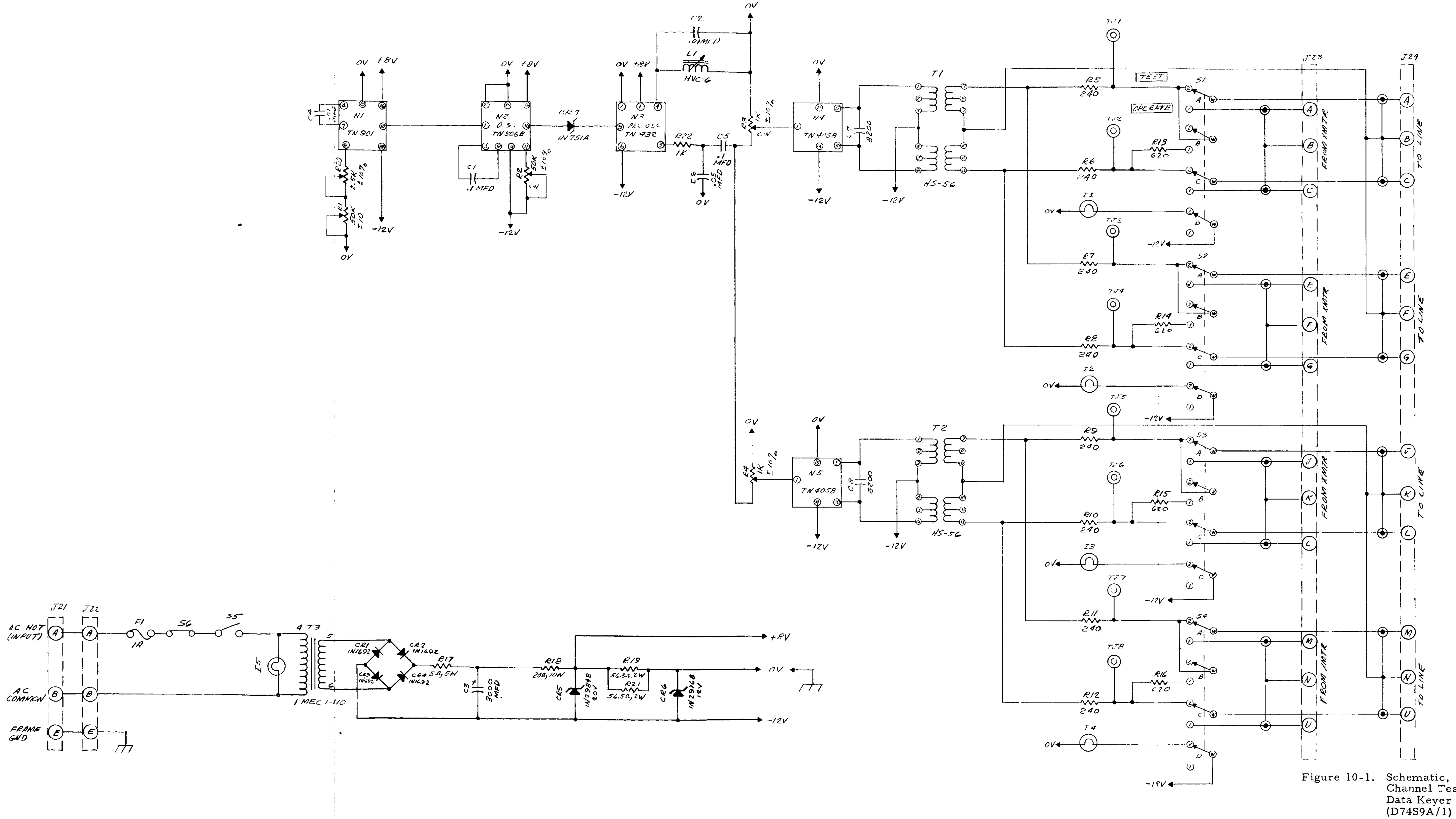
Step 9. Adjust R2 until the output has one cycle of 2 kc followed by a blank space followed by one cycle of 2 kc, etc.

Step 10. Using R1 as a coarse adjustment and R20 as fine, adjust the frequency of N1 until the EPUT Meter reigsters 1 kc.

Step 11. Readjust R2 until the optimum signal appears on the scope (no severe discontinuities, etc.).

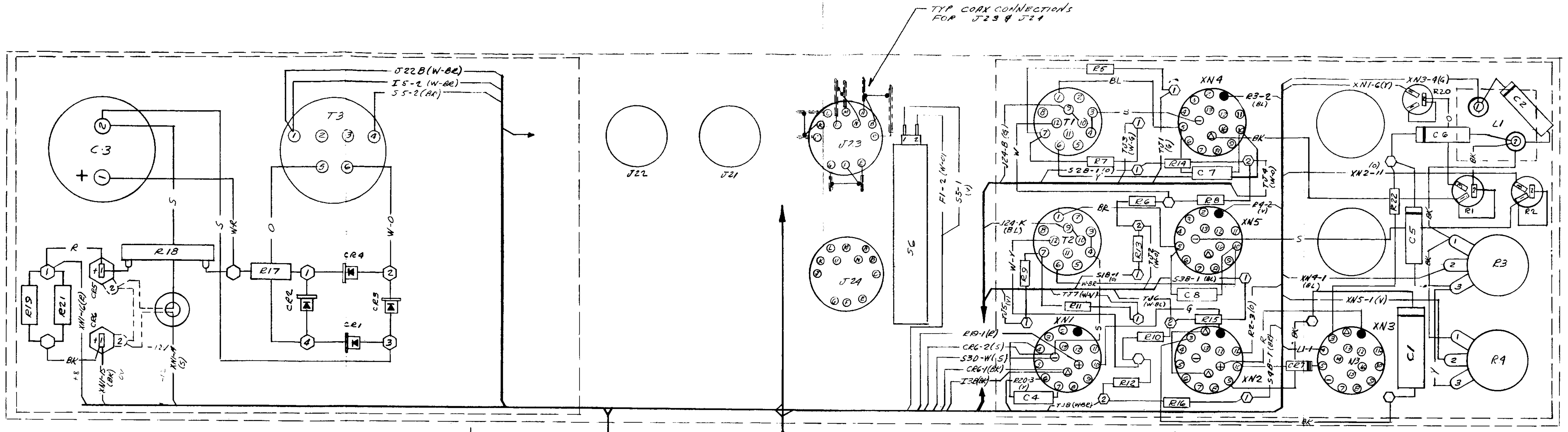
Step 12. Place the oscilloscope leads on TJ6 and TJ7. Adjust R4 until the desired output level is reached.

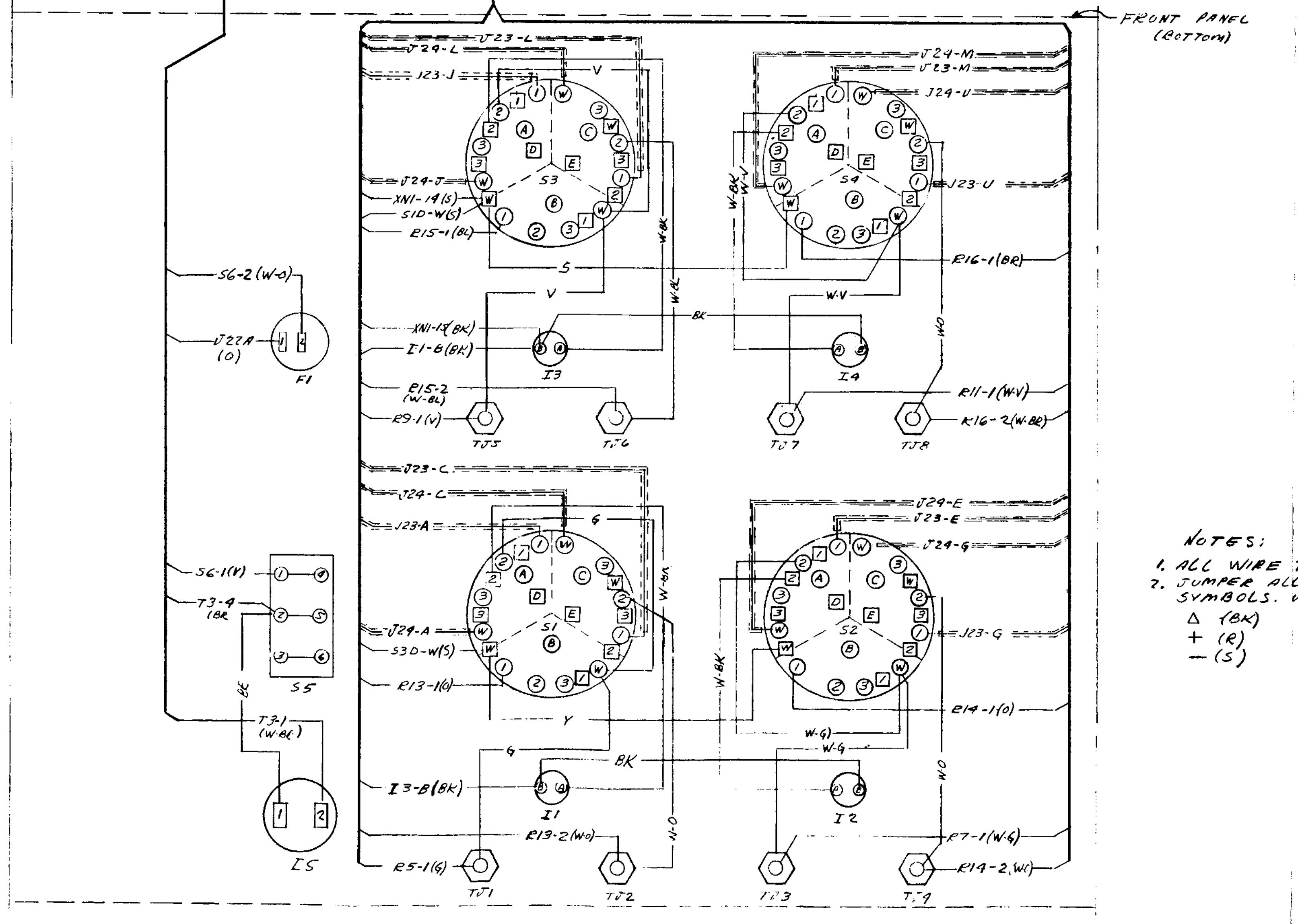
Step 13. When any of the Data Transmitter switches are placed in the OPERATE position, the Model 71-12A Keyer corresponding to that switch will output directly to the telephone line.



NOTES:
1. ALL RESISTORS ARE 1/2 W ± 5% UNLESS OTHERWISE SPECIFIED

Figure 10-1. Schematic, Four Channel Test Data Keyer (D74S9A/1)





J21			
PIN	DESTINATION	FUNCTION	WIRE
A	J22-A	AC HOT	O
B	J22 B	AC COMMON	W-BR
E	J2L E	CHASSIS GND	BK

J22			
PIN	DESTINATION	FUNCTION	WIRE
A	F1-1	AC HOT	O
B	T3-1	AC COMMON	W-BR
E	GNG LUG	CHASSIS GND	BK

J23			
PIN	DESTINATION	FUNCTION	WIRE
A	S1A-1	FROM XMTR	COAX
B			
C	S1C-1	FROM XMTR	COAX
E	S2A-1	FROM XMTR	COAX
F			
G	S2C-1	FROM XMTR	COAX
J	S3A-1	FROM XMTR	COAX
K			
L	S3C-1	FROM XMTR	COAX
M	S4A-1	FROM XMTR	COAX
N			
U	S4C-1	FROM XMTR	COAX

J24			
PIN	DESTINATION	FUNCTION	WIRE
A	S1A-W	TO LINE	COAX
B	T1-9	TO LINE	G
C	S1C-W	TO LINE	COAX
E	S2A-W	TO LINE	COAX
F		TO LINE	
G	S2C-W	TO LINE	COAX
J	S3A-W	TO LINE	COAX
K	T2-10	TO LINE	BL
L	S3C-W	TO LINE	COAX
M	S4A-W	TO LINE	COAX
N		TO LINE	
U	S4C-W	TO LINE	COAX

NOTES:
1. ALL WIRE TO BE #22 GA UNLESS OTHERWISE NOTED
2. JUMPER ALL POINTS MARKED WITH THE FOLLOWING SYMBOLS, USING COLORS INDICATED
△ (BK)
+ (R)
− (S)

Figure 10-2. Wiring Diagram, Four Channel Test Data Keyer (D74W9A/1)

APPENDIX

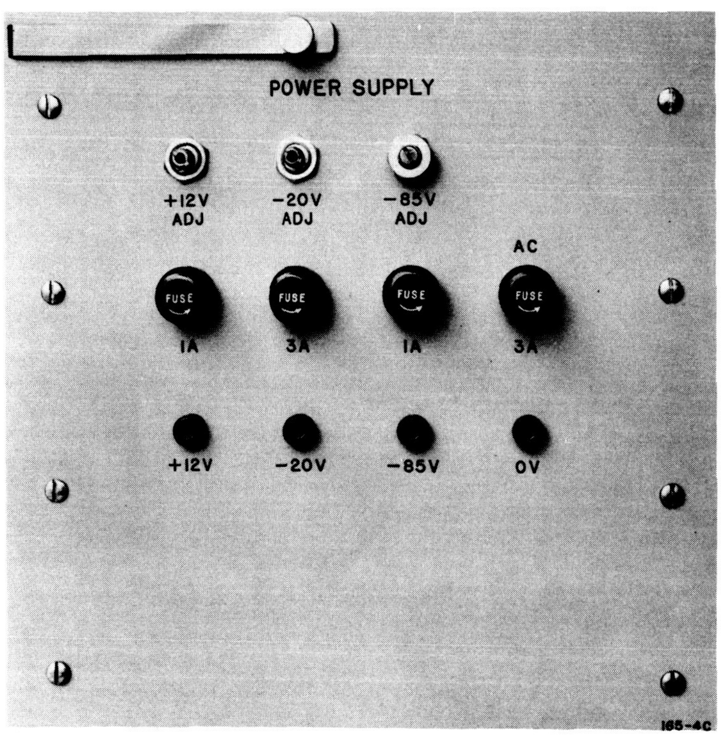
TRANSISTOR POWER SUPPLY
MEC MODEL 165-4 C

1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v (±5v) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.



Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414,and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

4. -65v SUPPLY

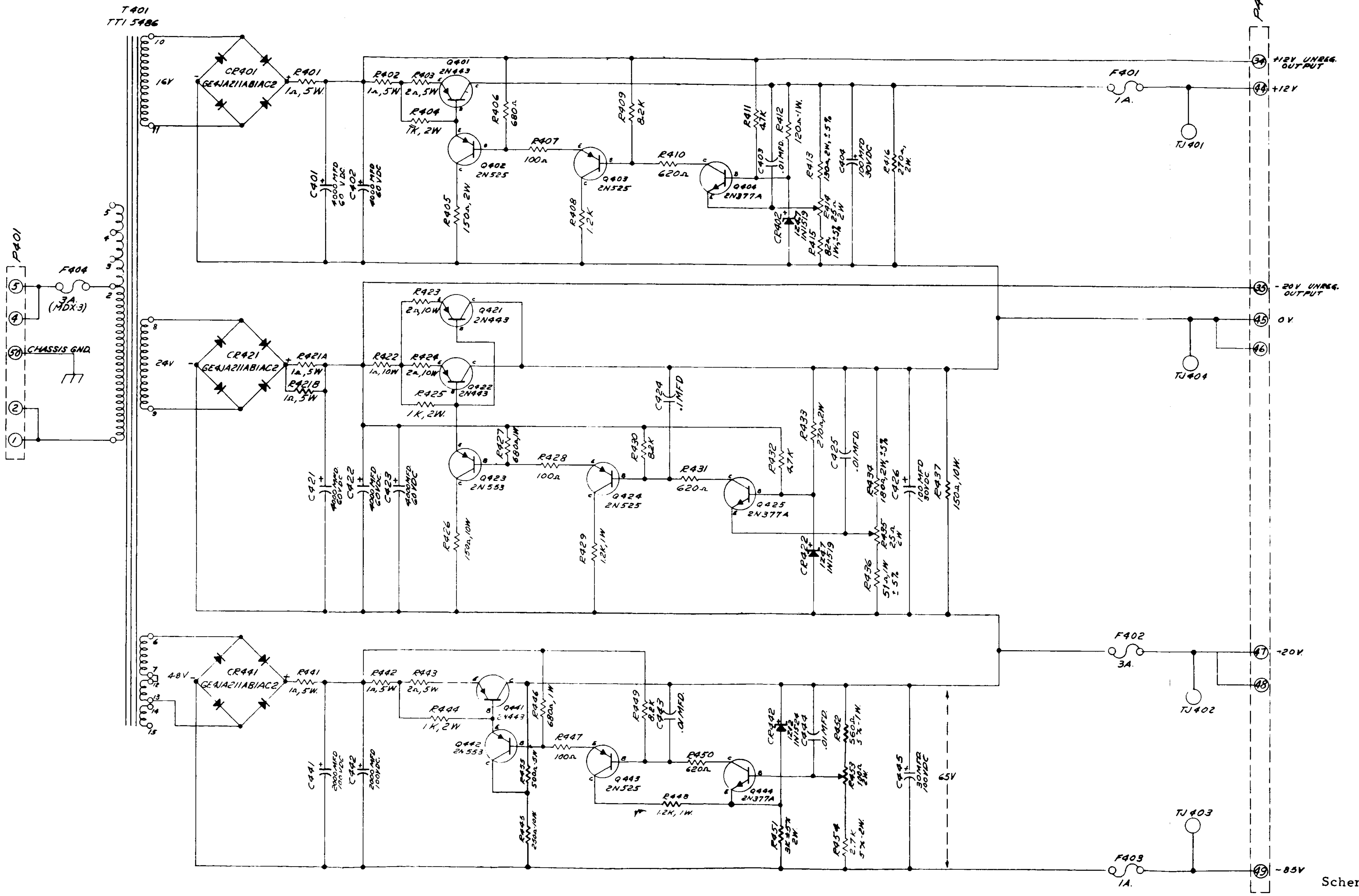
4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

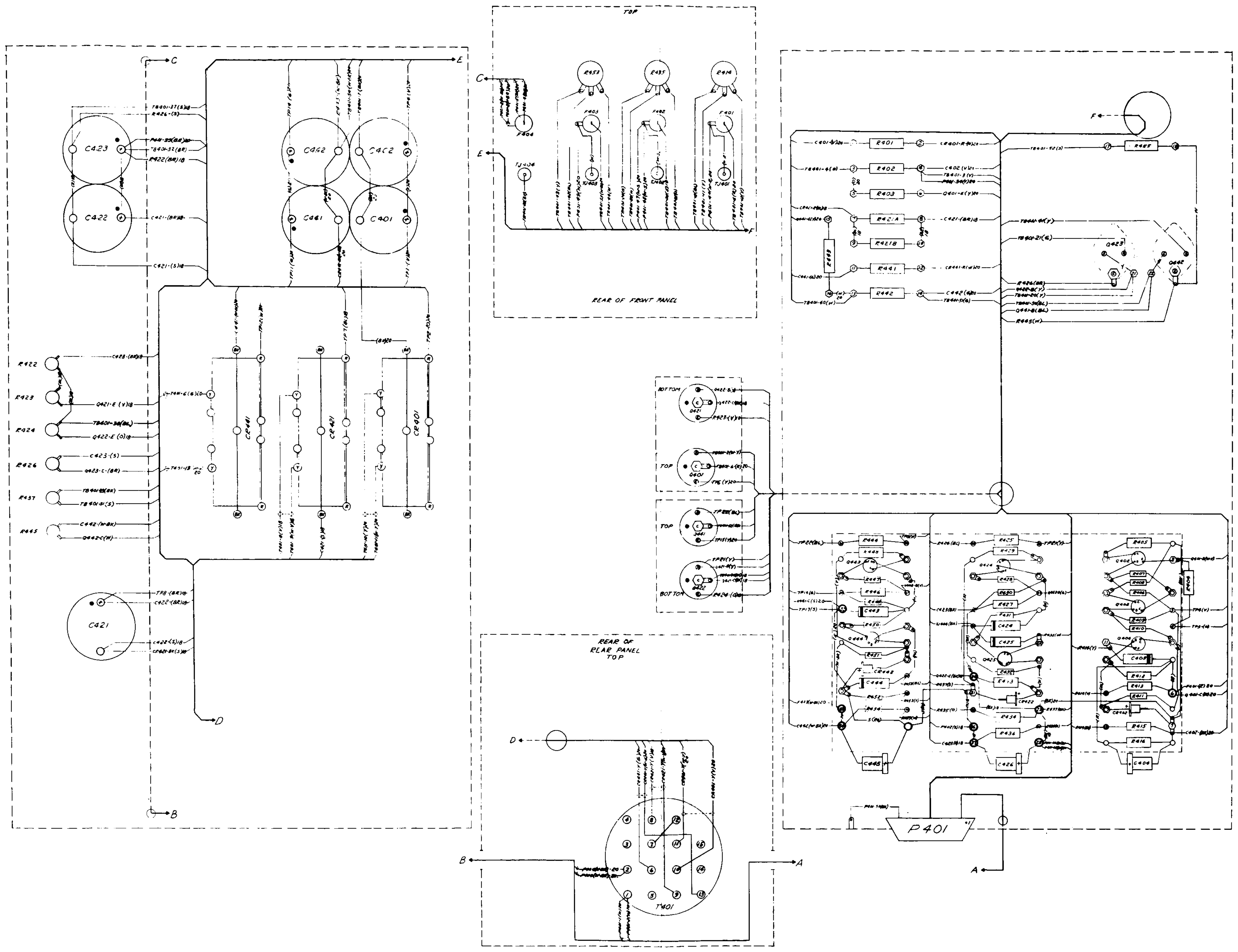
4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.



Schematic
165-4C Power Supply
Dwg. #D165S4C



P401							
PIN	DEST	FUNCTION	WIRE	PIN	DEST	FUNCTION	WIRE
1	T401-1	AC INPUT	(W) 20	41			
2	T401-1	AC INPUT	(W) 20	42			
3				43			
4	F404	AC INPUT	(BR) 20	44	F401	+12 V	(W-R) 20
5	F404	AC INPUT	(BR) 20	45	T401-25	0 V	(BK) 20
6				46	T401-25	0 V	(BK) 20
7				47	F402	-20 V	(W-S) 20
8				48	F402	-20 V	(W-S) 20
[illegible]	TP 4	[illegible]	(Y) 20	49	F403	-88 V	(W) 20
[illegible]	[illegible]	[illegible]	[illegible] 20	50	CHASSIS	CHASSIS GND	(BK)

NOTES:
1. ALL WIRE 22GA. UNLESS SPECIFIED
2. ALL AC. WIRES TO BE TWISTED IN PAIRS.

Wiring Diagram
165-4C Power Supply
Dwg. #E165W46

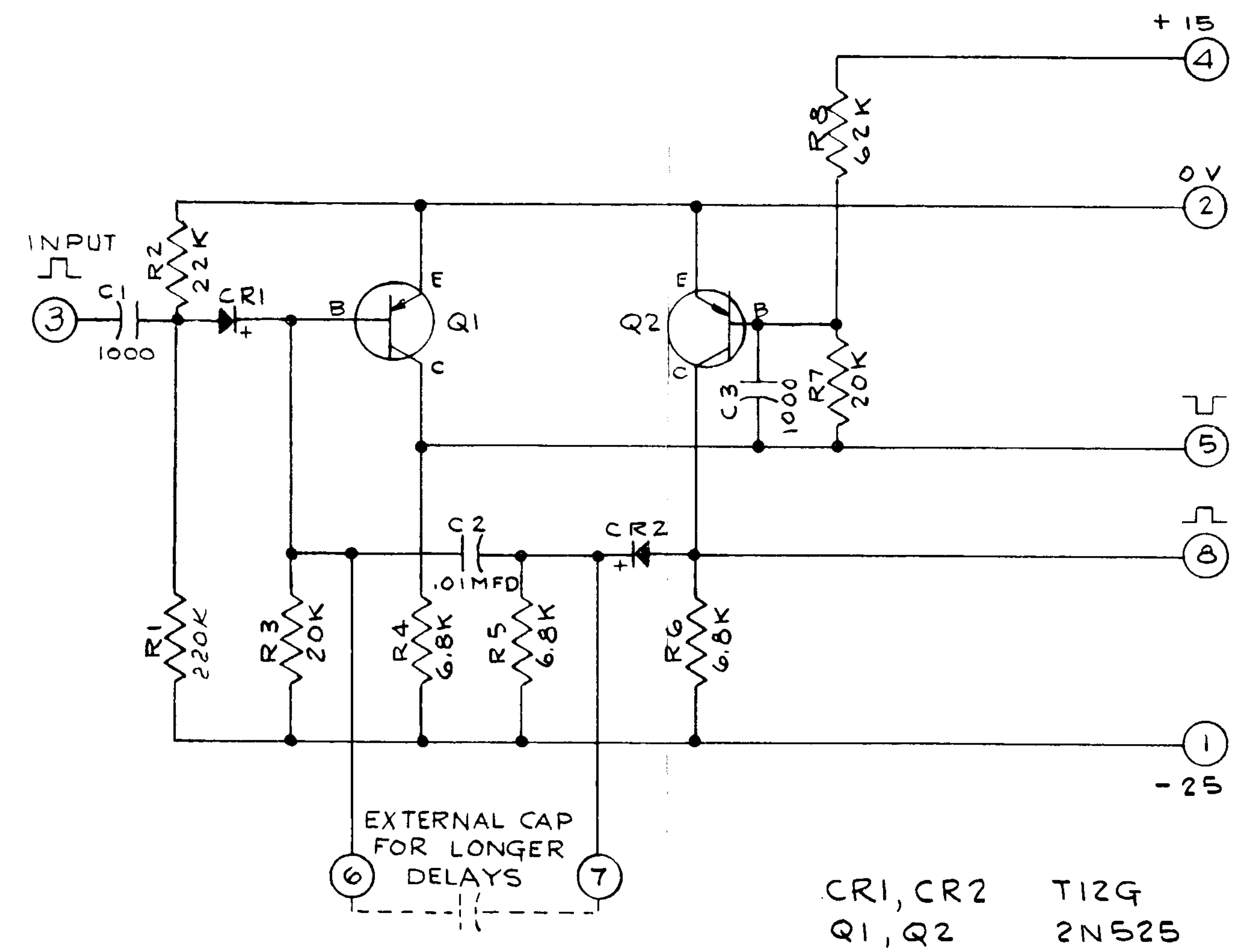
TN 51
ONE-SHOT (MONOSTABLE MULTIVIBRATOR)

The TN51 is a one-shot (monostable multivibrator) used for generating a pulse, variable in width from a minimum of 160 microseconds to over 2 milliseconds. In the quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage divider R7 and R8 is connected between +15 volts and 0 volts, establishing a positive reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network. A positive pulse of not less than 10 volts, with a rise time not greater than 4 microseconds, will trigger the network by cutting off transistor Q1. Transistor Q1 is cut off when the input pulse raises the base voltage of transistor Q1 above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts almost to 0 volts. This rise of voltage is coupled to the base of transistor Q2 via capacitor C2, keeping transistor Q1 at cut off until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return below 0 volts. Q1 saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 7 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for the current of C2., This network will operate on lower, supply voltages such as +12 volts and -20 volts, or +10 volts and -15 volts.



Schematic,

TN51 One-Shot (Monostable Multivibrator)

Dwg. #A103S51A

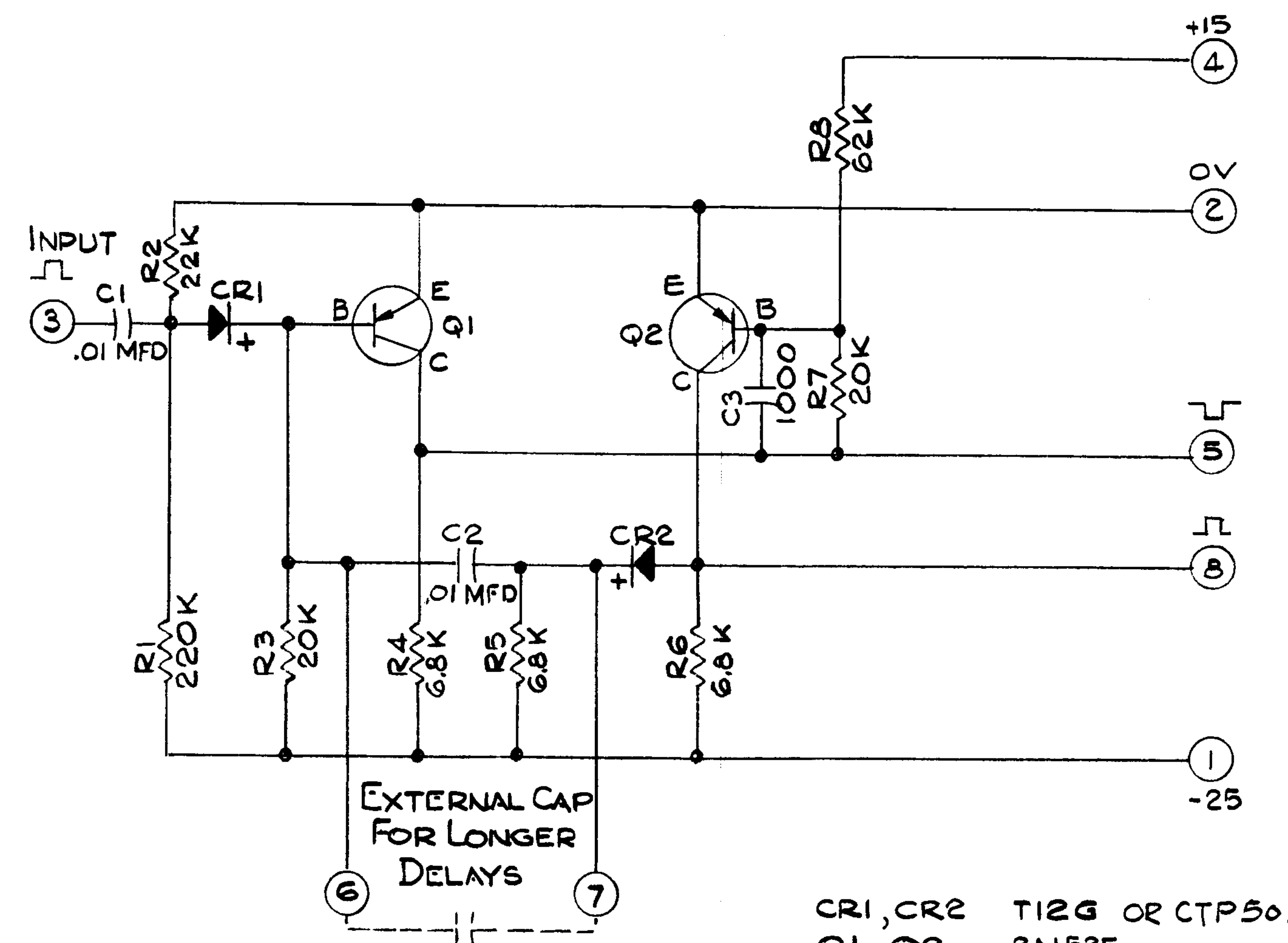
TN 51 B
MONOSTABLE FLIP-FLOP

A TN51B is a monostable flip-flop used for generating a pulse, variable in width from a minimum of 160 microseconds to over 2 milliseconds. In the quiescent condition, transistor Ql is saturated by the base current through resistor R3. Since transistor Ql is saturated, voltage divider R7 and R8 is connected between +15 volts and 0 volts, establishing a reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistor Rl and R2 form a voltage divider, establishing a noise bias of approximately -2. 5 volts, so that normal input noise does not trigger the network. A positive pulse of not less than 10 volts with a rise time not greater than 4 microseconds will trigger the network by cutting off transistor Ql. Transistor Ql is cut off when the input pulse raises the base voltage of transistor Ql above 0 volts. Capacitor Cl is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Ql cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts almost to 0 volts. This rise of voltage is coupled to the base of transistor Ql via capacitor C2, keeping transistor Ql at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Ql to return below 0 volts. Ql saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 7 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for the current of C2. This network will operate on lower supply voltages, such as +12 volts and -20 volts.



Schematic

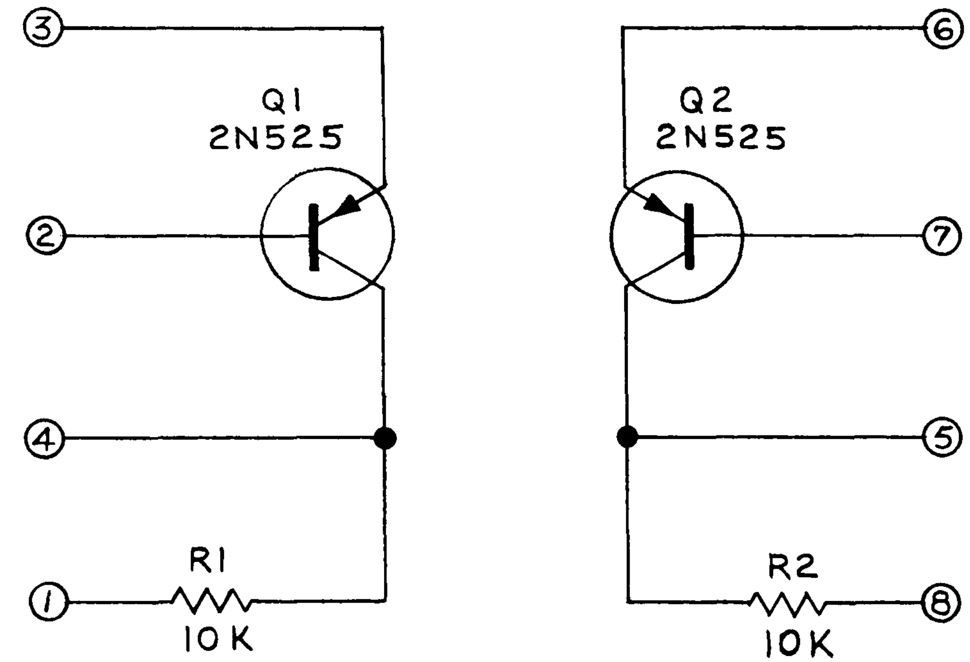
TN51B, Monostable Flip-Flop

Dwg. A103S51B

TN 57
DUAL PULSE AMPLIFIER

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.

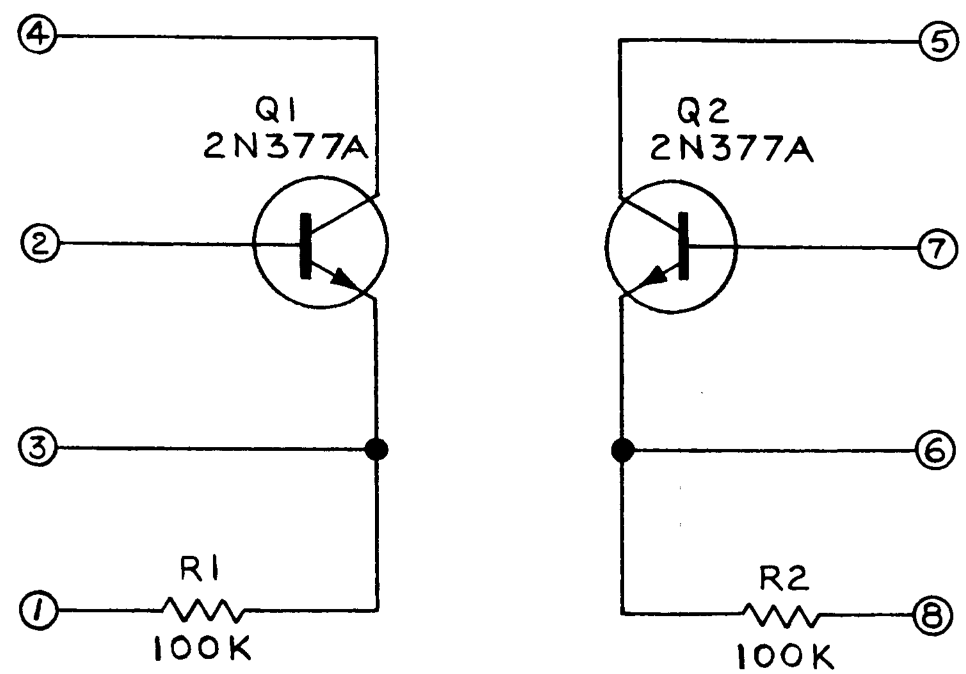


Schematic
TN57 Dual Pulse Amplifier
Dwg. #A103S57A

TN 58
DUAL EMITTER FOLLOWER

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.



Schematic
TN58 Dual Emitter Follower
Dwg. #A103S58A

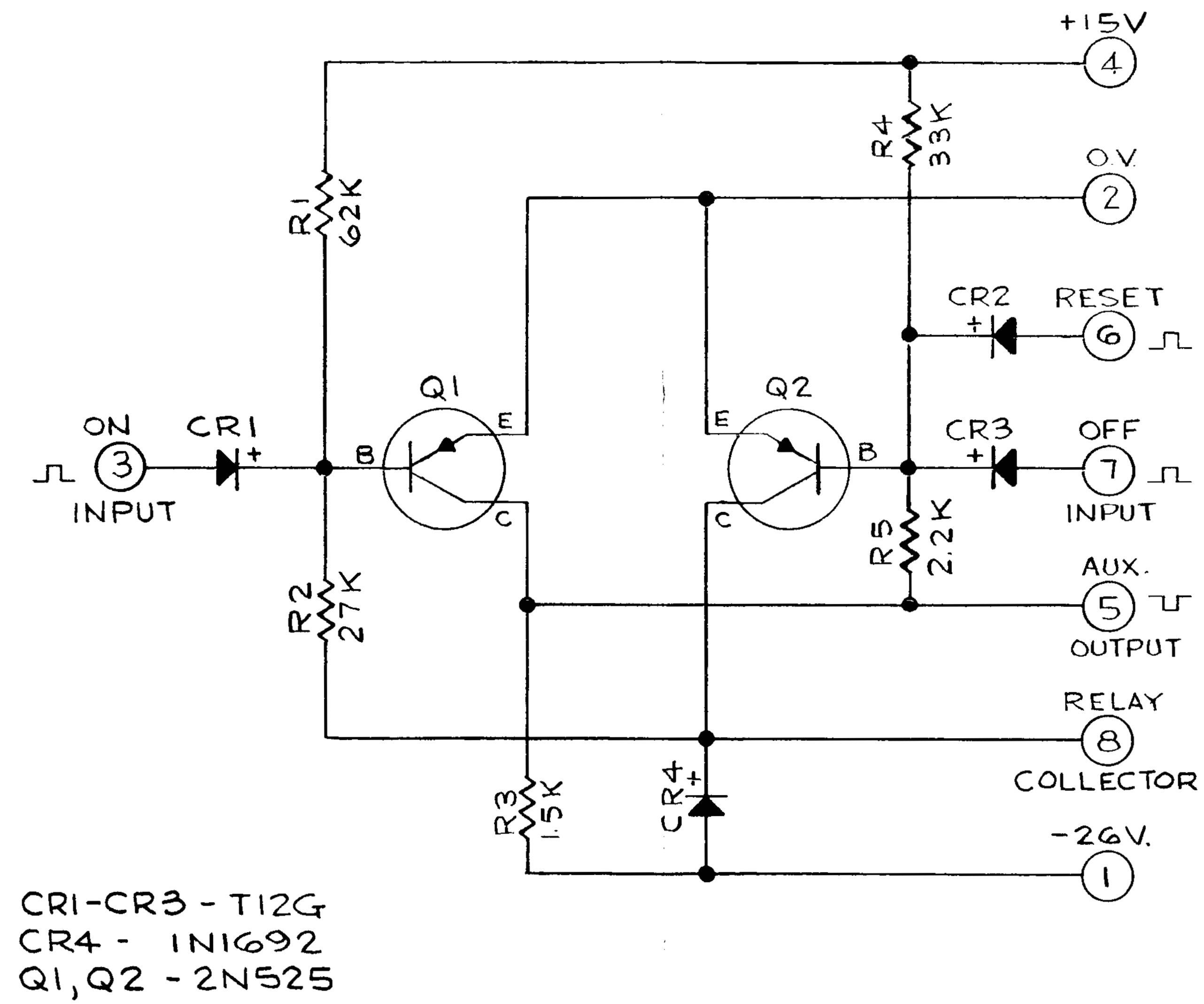
TN 79
RELAY DRIVING FLIP-FLOP

A TN79 is a bistable flip-flop which can be used for driving a relay coil (or other load) of 200 ohms or more. The external load is connected between pins 8 and 1. The network is normally said to be in the "Off" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "On", or "1", condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize.

If we assume that Q1 is saturated, then its collector is at approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base will be at approximately -0.5 volts, and the current through resistor R1 is approximately 0.25 ma. The current through the series combination of R2 and the external load resistor, which may vary from 300 ohms to 3K, will vary from 0.93 to 0.85 ma. The difference between the currents in R1 and in R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition; therefore, that condition is a stable one.

The input voltages at pins 3, 6, and 7 must be negative during quiescent conditions. The flip-flop may be turned "On" by raising the voltage at pin 3 to a positive value so the diode CR1 conducts, raising the base voltage of Q1 to a positive value. The input pulse will be loaded slightly and cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Resistors R1 and R2 are now connected from +15 volts to 0 volts, and hold the base of Q1 at approximately +4.5 volts, keeping Q1 in a cut off condition after the input pulses pass. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition.

Diode CR2 is included to suppress the external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cut off, the relay coil is de-energized. However, the inductance in the relay coil attempts to maintain the current through the coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil and eliminating the voltage spike. This network will operate on a lower supply voltage, such as +12 volts and -20 volts.



Schematic,

TN79 Relay Driving Flip-Flop

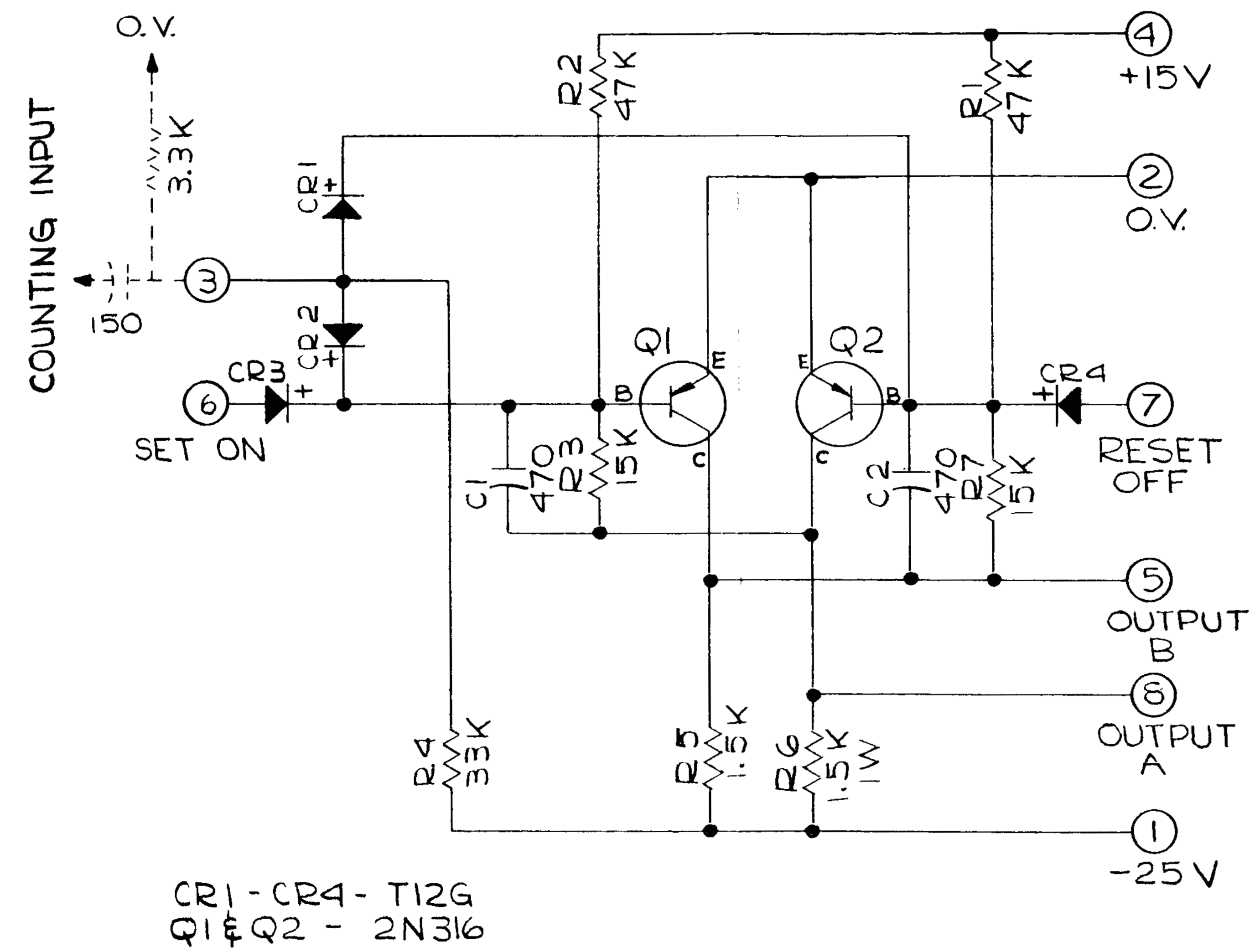
Dwg. #A103S79A

TN 90B

BALANCED FLIP-FLOP AND DIVIDER

The TN90B is a bistable balanced flip-flop. An auxiliary input (pin 3) allows the network to be used as a divider in a counter.

The network is defined as being in the "0" state when Q1 is saturated and Q2 is off and in the "1" state when the reverse is true. Assume that Q1 is saturated ("0" state) then the collector voltage of Q1 will be approximately 0 volts and resistor divider, R1 and R7, will maintain approximately +3.5 volts of reverse bias on the base of Q2, keeping it cut off. With Q2 cut off, resistors R3 and R6 will provide a path for Q1 base current, clamping Q1 in saturation. This condition is stable and will not be changed until an input is received on pin 3 or pin 6. Pin 6 is in "1" input, in that a positive pulse above 0 volts at pin 6 will cause CR3 to conduct, thus driving the base of Q1 positive above 0 volts, reverse biasing Q1, subsequently cutting Q1 off. As Q1 is cut off its collector will go negative and due to the resistor divider, R1 and R7, the base of Q2 will go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and due to the resistor divider of R2 and R3 the base of Q1 will be reverse biased at approximately +3.5 volts, keeping Q1 cut off, after the input pulse has passed. The network will remain in the "1" state until reset by a positive pulse on pin 7 or triggered from a pulse on pin 3, the counting input. If a positive pulse is applied on pin 3 through an external capacitor for differentiation, both Q1 and Q2 will be cut off. Capacitors C1 and C2 retain charges which are dependent upon which one of the transistors was saturated before the input pulse occurred. Since the input pulse is differentiated by a small input capacitor, it will last a very short time, less than one microsecond. At this point, the internal capacitors C1 and C2 take over, turning on the transistor that had previously been off. For example; assume the network is the "1" state, therefore Q1 is cut off and Q2 is saturated. The voltage across C1 will be approximately 3.5 volts and across C2 will be approximately 26 volts. When pin 3 goes positive above 0 volts, both bases will be driven positive, cutting the transistors off. The collector of Q2 starts to go negative from 0 volts to -23 volts. Since this occurs almost instantaneously and C1 has been charged only 3.5 volts the base of Q1 will go negative, turning Q1 on. As Q1 is turned on, Q2 is held cut off and we are now in the "0" state as explained previously. Note, since the collector of Q1 was at -23 volts before the pulse occurred on pin 3 and there wasn't any change of collector voltage when the pulse did occur. The base of Q2 would not experience any change through C2. The output pins of the network are 5 and 8. When the network is in the "0" state pin 5 will be at 0 volts and pin 8 will be approximately -23 volts and the reverse is true when the network is in the "1" state. Although the description of operation has been based on voltages of +15 volts and -25 volts this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.



Schematic,

TN90B Balanced Flip-Flop and Divider

Dwg. #A 103S90B

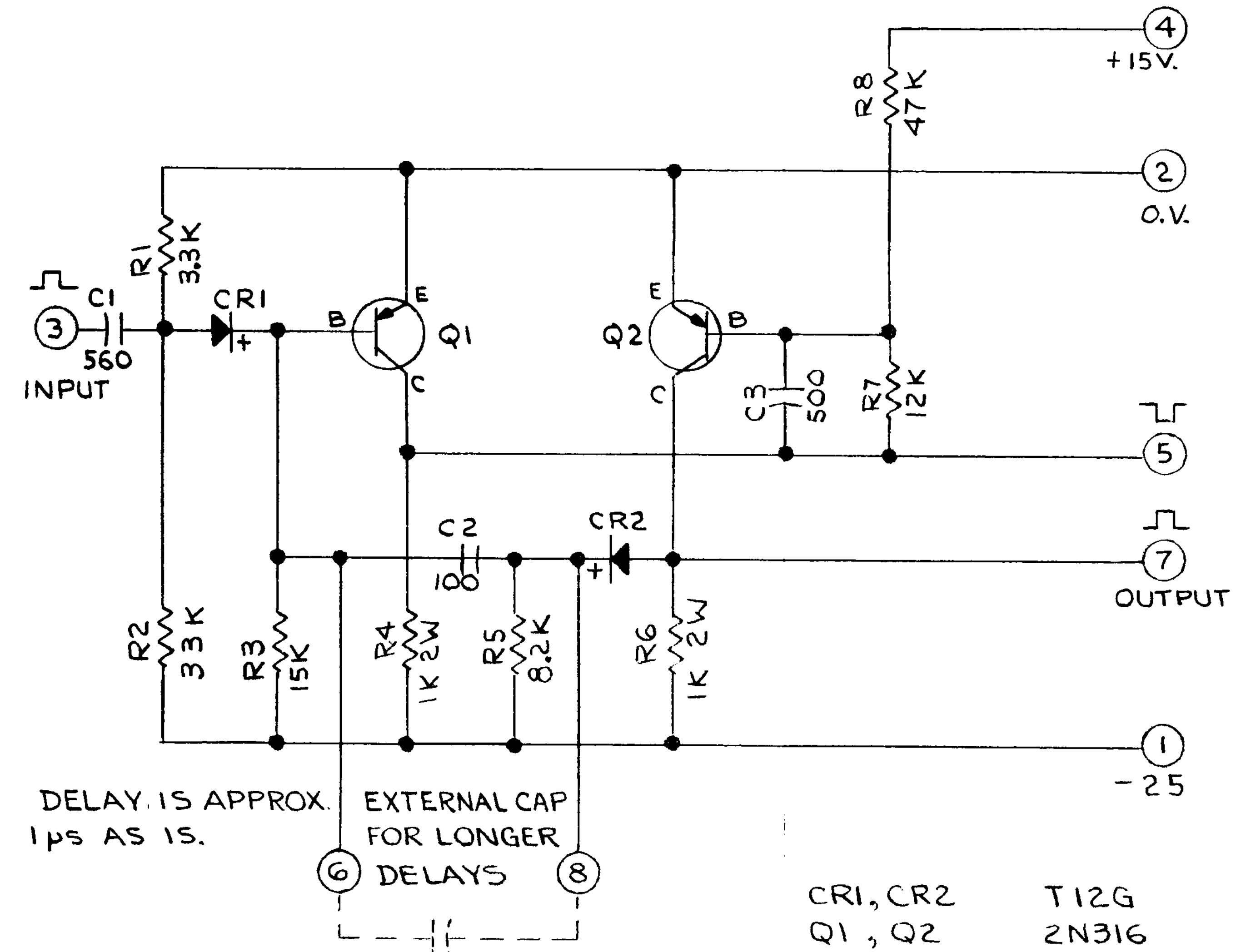
TN 111
ONE-SHOT (MONOSTABLE MULTIVIBRATOR)

The TN111 is a one-shot (monostable multivibrator) used for generating a pulse which can be varied from a minimum of one microsecond to well over 200 microseconds. In the quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage divider R7 and R8 is connected between +15 volts and zero volts, establishing a reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise will not trigger the network. A positive pulse of not less than 10 volts, with a rise time not greater than 0.5 microseconds, will trigger the network by cutting off transistor Q1. Transistor Q1 is cut off when the input pulse raises the base voltage of transistor Q1 above zero volts. Capacitor C1 is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to almost zero volts. This rise in voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than zero volts. Q1 saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a dc path for the current of C2. This network will operate on lower power supply voltages, such as +12 and -20 volts, or +10 and -15 volts.



Schematic,

TN111 One-Shot Monostable Multivibrator

Dwg. #A103S111A

TN 130 B
CORE DRIVER

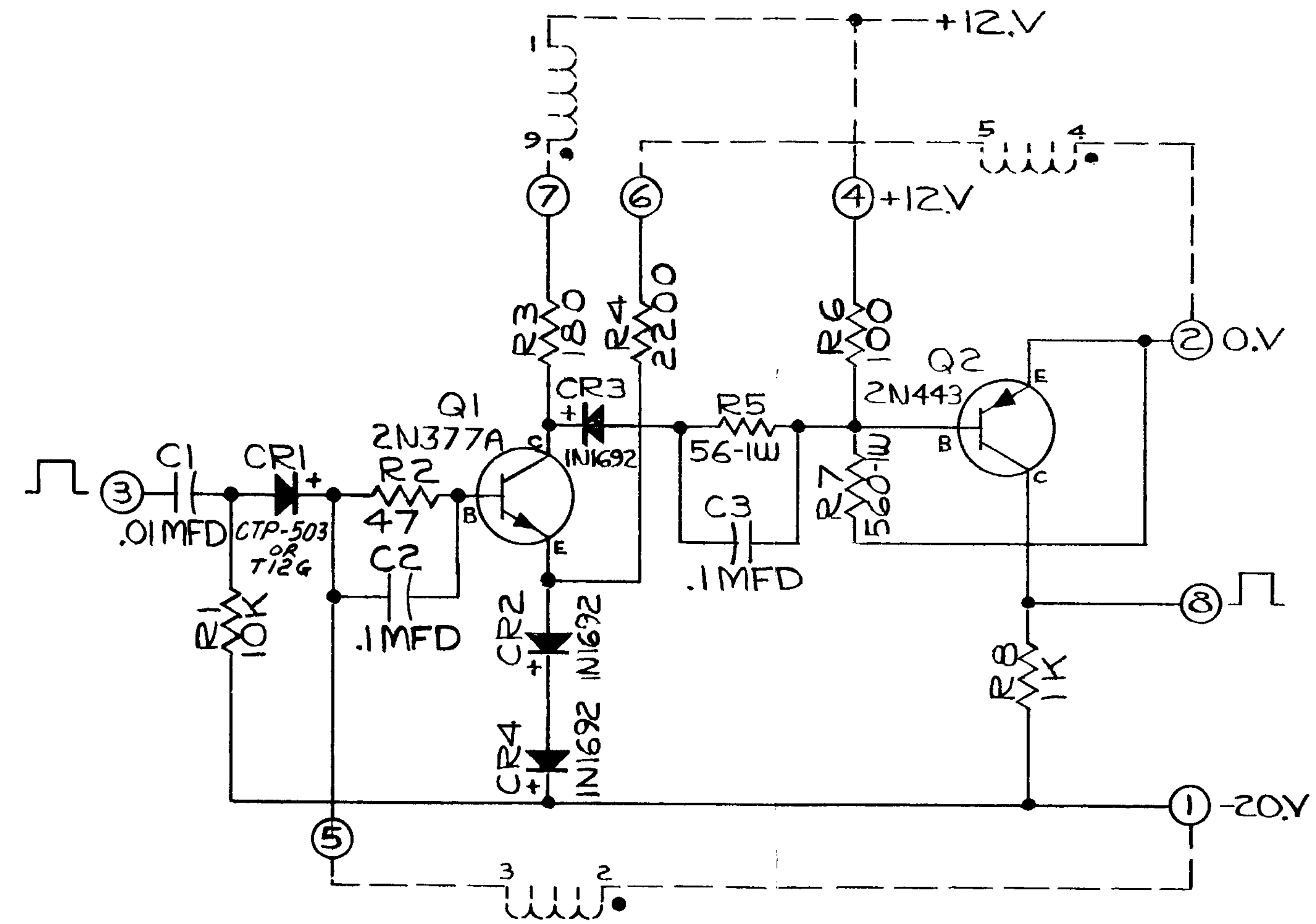
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).



NOTE:
ALL RESISTORS ½ WATT ±10%
UNLESS OTHERWISE NOTED.

Schematic,

TN130B Core Driver

Dwg. #A103S130B

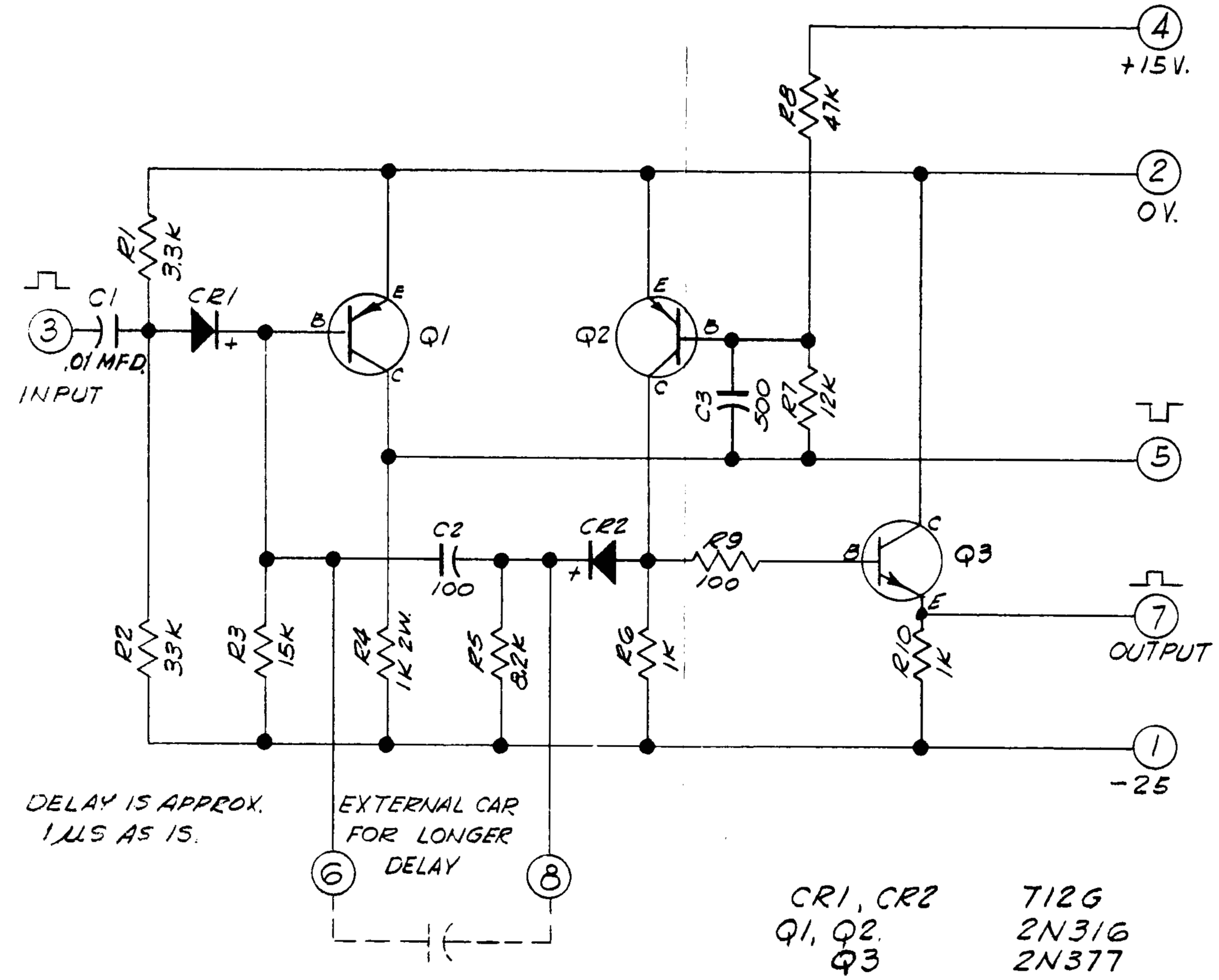
TN 138
ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138 is a monostable flip-flop used for generating a pulse which can be varied in width from a minimum of about 2 microseconds to over 200 microseconds. In quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage dividers R7 and R8 are connected between +15 volts and 0 volts, establishing a positive bias voltage on the Q2 base, and keeping Q2 cut off. Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network.

A positive pulse of not less than 10 volts, with a rise time not greater than 1 microsecond, will trigger the network by cutting off transistor Q1. Q1 is cut off when the input pulse raises the base voltage above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to nearly 0 volts. This rise of voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than 0 volts. Q1 now saturates again and cuts off Q2. This time can be lengthened by adding capacitance in parallel with capacitor C2.

The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for current of C2. Q3 is the emitter-follower which will drive a load of 200 ohms.



Schematic
TN138
Dwg. #A103S138

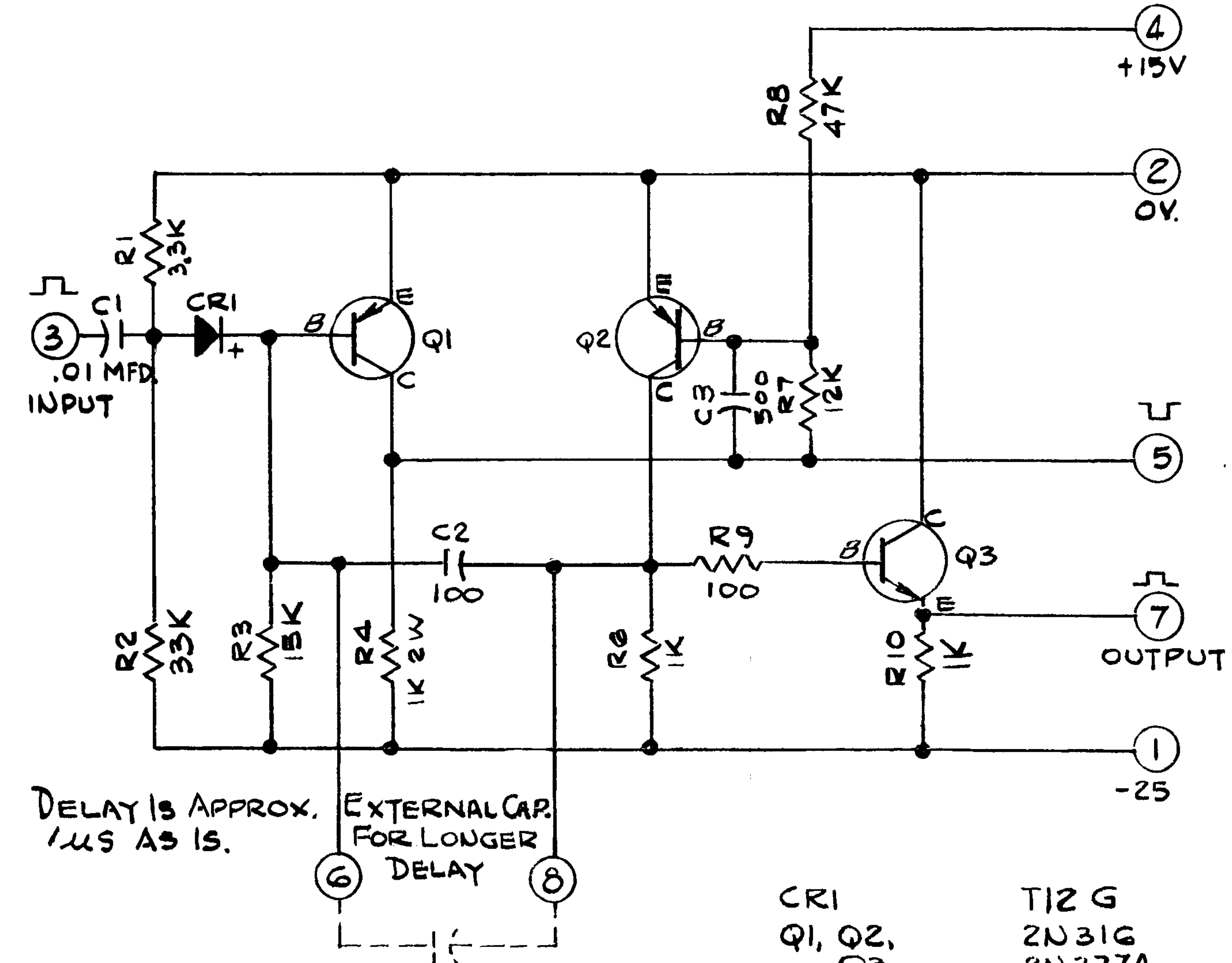
TN 138 B
ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138B is a one-shot (monostable multivibrator) with an emitter follower output. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated and with Q2 cut off. The base of Q1 is forward biased by R3 which is connected to -25 volts, thus saturating Q1. Since Q1 is saturated, the base of Q2 is reverse biased by the voltage divider R7 and R8 between +15 volts and the collector of Q1 (0 volts). With Q2 cut off, its collector is at approximately -25 volts; therefore the base of Q3 is at the same voltage as the emitter of Q3, keeping Q3 near cut off. Pin 7 will be at -25 volts and pin 5 will be at 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2.2 volts for protection against noise impulses. When a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -25 volts. This negative going voltage potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will now conduct, and starts to saturate rapidly. The collector of Q2 will now go positive from -25 volts to 0 volts. This voltage change, being coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive. Due to the resistor divider of R7 and R8, the base of Q2 will also go positive, reverse biasing Q2 and cutting it off. The one-shot has now returned to its quiescent condition.

The time constant of R3 and C2 determines the pulse width, which is about 1 microsecond. By adding external capacity across pins 6 and 8, the RC time constant is increased and thus the pulse width is increased. When Q2 is saturated, the base of Q3 will be positive in respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will go to 0 volts. Q3 will be in saturation as long as Q2 is in saturation. When Q2 is cut off, Q3 will be near cut off, and pin 7 will return to -25 volts.

Although the description of operation has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +10 volts and -15 volts.



Schematic,

TN138B One-Shot with Emitter Follower Output

Dwg. #A103S138B

MAGNETIC CORES

1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

2. THEORY OF OPERATION

2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on the hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

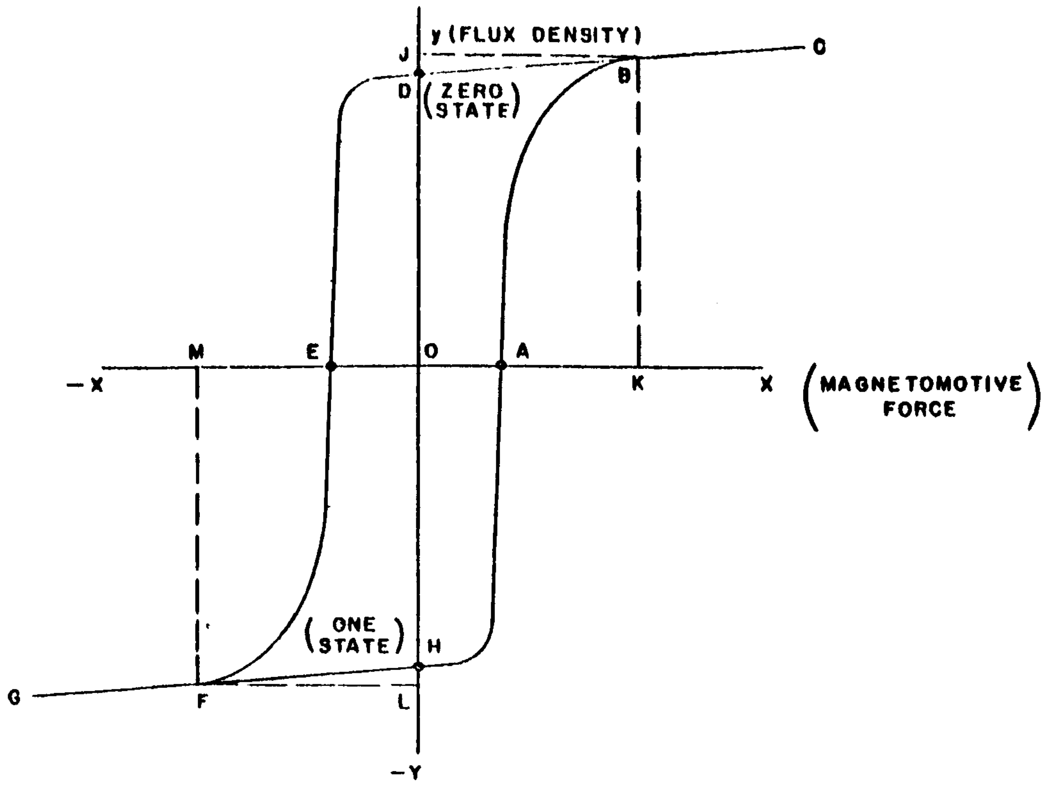


Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

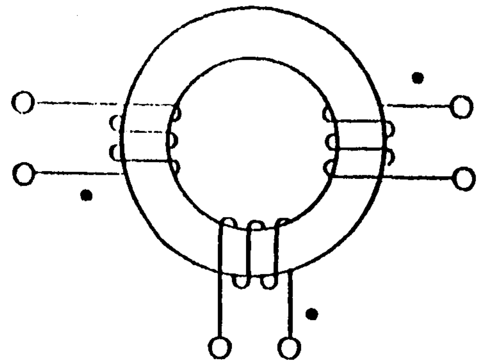


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to DL. The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "O" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one C3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive-going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.

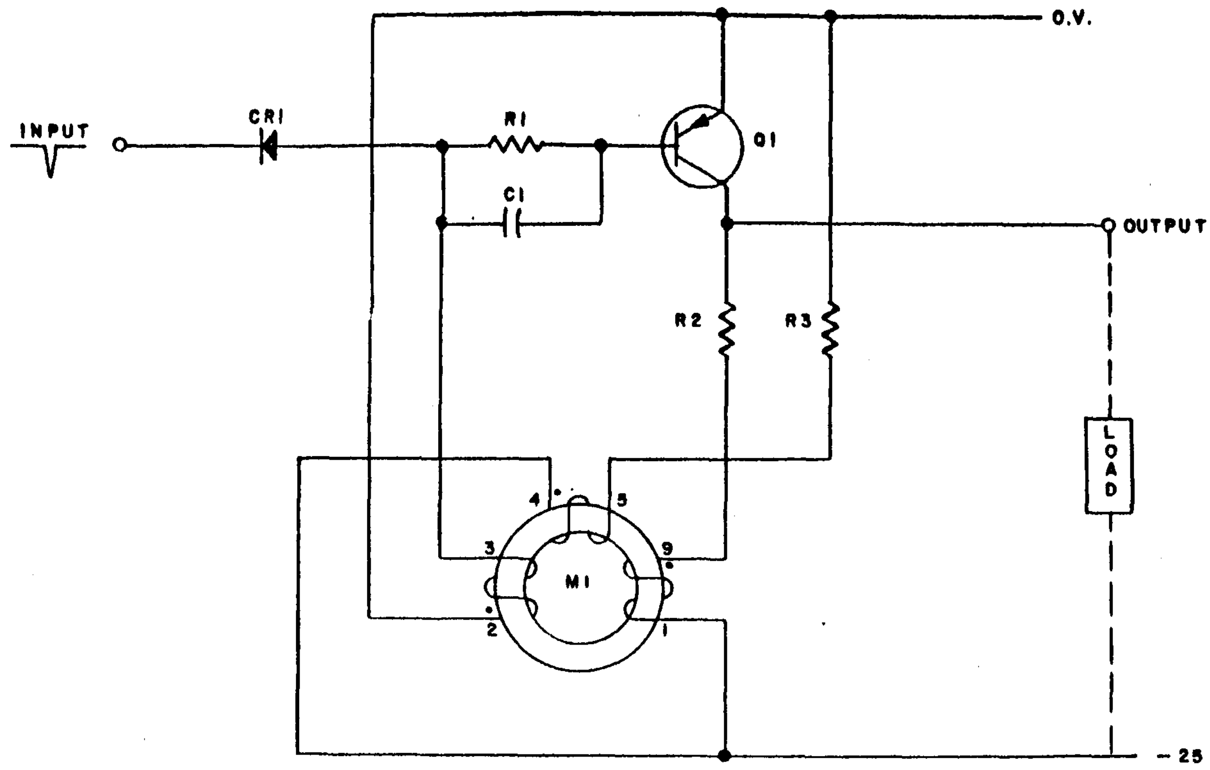


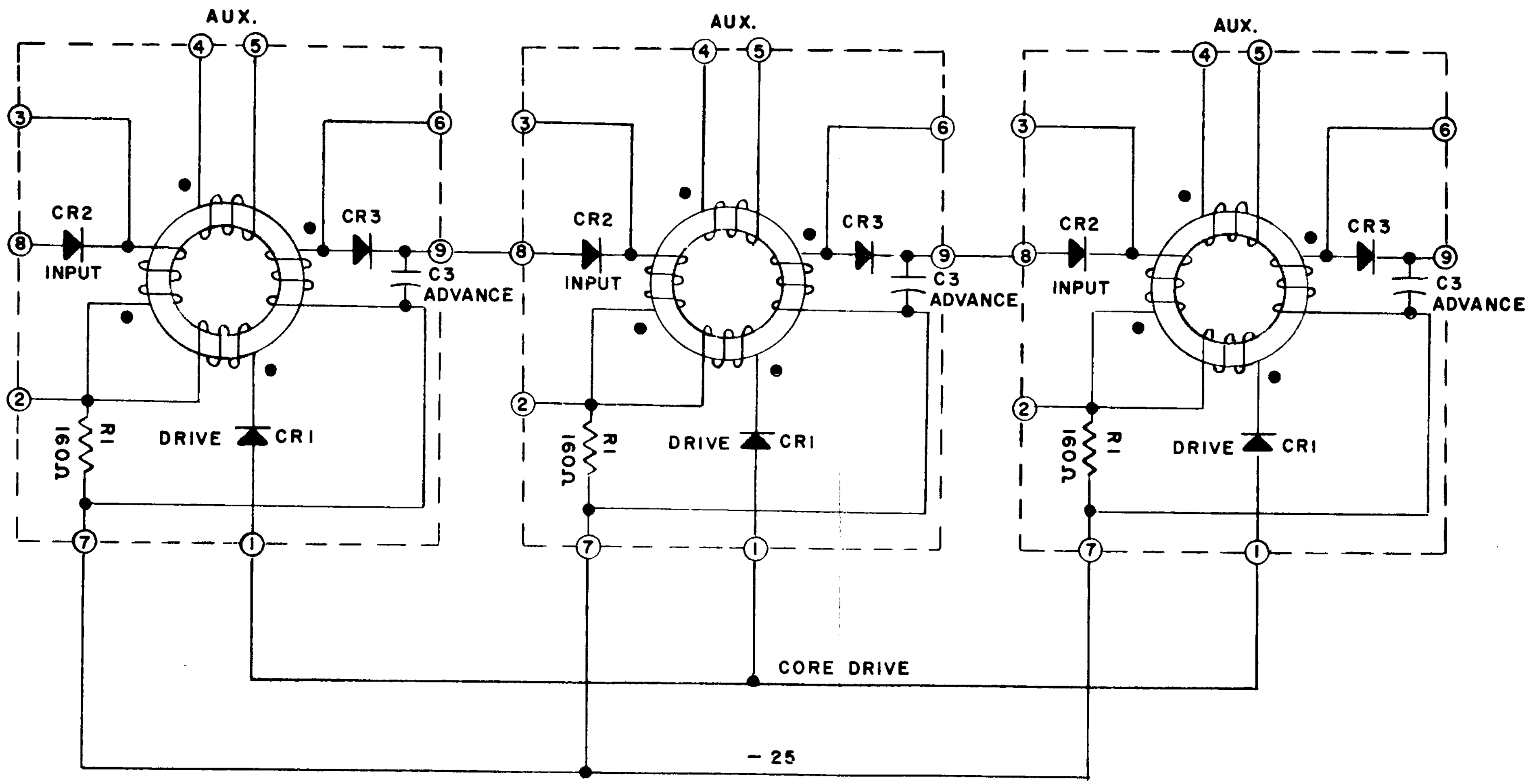
Figure MN-4. Blocking Oscillator (MN12 or MN13)

b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN13 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.


AUX.
4
5
3
6
CR2
CR3
8
9
INPUT
C3
ADVANCE
2
R1
160Ω
DRIVE
CR1
7
1
AUX.
4
5
3
6
CR2
CR3
8
9
INPUT
C3
ADVANCE
2
R1
160Ω
DRIVE
CR1
7
1
AUX.
4
5
3
6
CR2
CR3
8
9
INPUT
C3
ADVANCE
2
R1
160Ω
DRIVE
CR1
7
1
CORE DRIVE
- 25

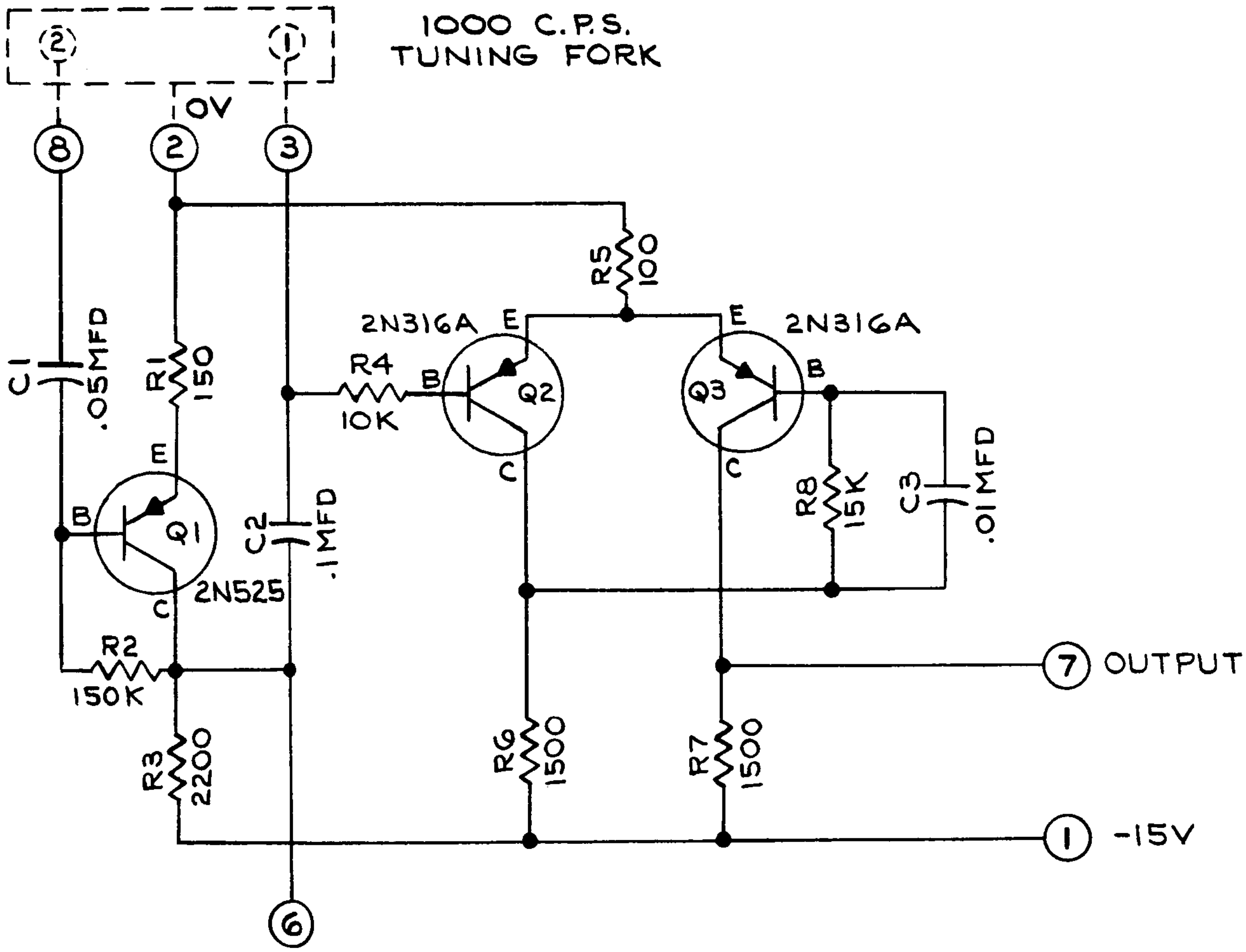
TN157
TUNING FORK OSCILLATOR

The TN157 is a transistor oscillator which is frequency controlled by an external tuning fork. The circuit is designed for use with a 1000 cps tuning fork, but operation is extended to include a 480 cps tuning fork by the addition of an external capacitor between pins 3 and 6.

A signal at the input, pin 8, is capacity coupled to the base of Q1, which amplifies the signal. The output of the first stage of amplification, pin 6, is coupled through C2 to the tuning fork and the output amplifier consisting of Q2 and Q3. As a result of being driven by Q1, the tuning fork resonates, providing the desired frequency at the pin 8 input.

Transistors Q2 and Q3 are used in a Schmitt trigger circuit which produces a saturated square wave output for a sinusoidal input to R4. As the input at the base of Q2 goes negative, turning on the transistor, its collector goes positive, turning off Q3. This positive feedback also exists in the case where the input to Q2 goes positive, generating the desired square wave output.

A warm up period is required for the oscillations to build up to maximum amplitude. This is due to the mechanical characteristics of the tuning fork. The warm up period may vary from 15 seconds to approximately two minutes.



NOTES:
1. ALL RESISTORS ± 10%, 1/2 WATT UNLESS NOTED.
2. ADD APPROXIMATELY A .5MFD CAPACITOR BETWEEN PINS 3 & 6 FOR A 480 C.P.S. TUNING FORK.

Schematic, TN-157. Dwg. #103S157A